

Design of a Grid Connected Photovoltaic Power Electronic Converter

MSc. Thesis

Advisors

Lars Norum Bjarte Hoff

Author

Mohsin Noman Mustafa



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Abstract

In this thesis, the designing of a grid-connected photovoltaic system for the power electronic laboratory of UiT- Campus Narvik has been carried out. The relevant topics and literature regarding the elements in a photovoltaic system and grid connection standards have been studied and reviewed. A system, with the capacity and ratings of solar modules currently available in the laboratory, has been designed in Simulink. The designed system in a multistage system. Perturb and Observe algorithm is used for maximum power point tracking. Boost converter is used to amplify the photovoltaic array voltage. The inverter used is a three-phase two-level inverter. The control structure for inverter is designed in synchronous reference frame. PLL extracts the necessary information of grid voltage phase. The grid has a Line to Line voltage of 400Vrms. An LCL filter is used to interconnect inverter output to the grid.

After that the results of the designed simulation are discussed. Hardware specific models are then made for code generation using the Embedded Coder feature of Simulink. In the end, discussion about this thesis, conclusion and recommendations for future work are presented.

to my parents

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List of Acronyms

AC	Alternating Current
ADC	Analog to Digital Converter
CC	Current Control
DC	Direct Current
DSP	Digital Signal Processing
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
МО	Modulus Optimum
MPPT	Maximum Power Point Tracking
P&O	Perturb and Observe
PWM	Pulse Width Modulation
SO	Symmetrical Optimum
SPWM	Sinusoidal Pulse Width Modulation
SVM	Space Vector Modulation
TI	Texas Instruments
VC	Voltage Control

List of Symbols

C_b	Base Capacitance
C_{pv}	Capacitor across PV array output
C _{DC Link}	DC Link Capacitor
C_{f}	Capacitor in LCL filter
D	Duty Cycle

f des PWM	Desired frequency of inverter PWM
f sys clk	Clock frequency of DSP Controller
i_d	D-axis Current
I_q	q-axis Current
Ir	Irradiance
L _{boost}	Inductor in Boost Converter
Li	Inverter side Inductor of LCL filter
L_g	Grid side Inductor of LCL filter
т	Modulation Index
<i>M(s)</i>	Current Control Loop Transfer Function
N(s)	Voltage Control Loop Transfer Function
Р	Power
T_i	LCL Filter Time Constant
T _{inv}	Inverter Time Constant
T _{int}	Integral Time Constant
V _{d_des}	D-axis Desired Voltage
V_{q_des}	Q-axis Desired Voltage
V _{d_mes}	D-axis Measured Voltage
V_{q_mes}	Q-axis Measured Voltage

1 Introduction

This chapter lays the foundation for this dissertation. It explains the motivation for this project as to why this project was needed. It also explains the objectives of the thesis and the organization of this report.

1.1 Background

In the past decade or so, focus has shifted towards obtaining energy from renewable resources rather than from fossil fuels. This has led to the commencement of wide scale research in the fields of wind and solar energy as these never-ending resources provide clean and sustainable energy with minimal pollution. Many countries want to shift completely on renewable energy by the next few years.

Wind power systems are generally employed for large scale power production in the form of wind farms, which are usually situated far from civilization as they produce noise [1] which may decline the quality of life for people residing nearby [2].

Solar PV systems, on the other hand, can be found ranging from a few hundred watts to MW capacity. This means that PV systems can provide energy solutions for individual houses. Tesla, a leading name in the companies that provide renewable solutions have even come up with a bright idea of providing solar roofs which will be available by the summer of 2017 [3].

Solar power systems are becoming more and more common because of their not too complex small scale system deployment. Places, where grid connection is not possible, make use of PV systems with backup batteries which can also provide electricity during night time when sunlight is not available.

Research areas that are nowadays focused for solar power systems include the design of the inverter, material of the modules and reliability of the system, among others.

1.2 Motivation

Renewable energy systems are the future of electric power generation systems. This being the case, both graduate and undergraduate studies of electric power should provide practical knowledge about the architecture of solar PV power generations systems. This has led to the conception of this dissertation. A system that can easily be modified for the purpose of experimentation, should be at disposal in the laboratory.

A system designing technique called Model Based Design [4] is gaining massive success as it leads to rapid prototyping. It provides the pathway through which the designed model can be used to generate code and that code can be fed into the system controller. Industries are replacing their generic designing techniques with Model Based Designing as it cuts the development time significantly [5]. Model Based Designing is possible through MATLAB as it provides the groundwork for it. Embedded Coder [6] by MATLAB is used for this purpose, which provides controller specific code which can be flashed into the dsp controller.

Workflow of MBD is shown in the figure below:



Figure 1.1: Model Based Design Workflow [4]

This designing technique provides an engineer with all the right tools as a system can be tested and code can be verified at every stage of the development process, not just after modelling the complete system.

1.3 Objectives and Goals

The main goal of this thesis is to model a PV system that can be used in the power electronics laboratory of UiT – campus Narvik, by using the code generation capability of Matlab and Simulink. The model would be target specific (for Texas Instuments dsp controller).

The task is divided into smaller objectives which need to carried out in order to achieve the goal. These objectives are:

- Review of photovoltaic systems.
- Review of Maximum Power Point Tracking Techniques.
- Understanding of inverter topologies.
- DC-DC converter modelling and simulation.
- Review of Inverter types.
- Modelling and simulation of DC-AC inverter and its control.
- Simulation of the overall system.
- Selection of DSP controller from Texas Instruments.
- Model Based designing of the PV system and code generation using Simulink library for Texas Instruments C2000 microcontrollers.
- Hardware Implementation of the whole system by using the code generated by Simulink (if time is available).

1.4 Structure of the Report

Chapter 2 of this report presents literature review of the PV system. It provides knowledge about single stage and multistage PV systems. This chapter explains the need of MPPT and mentions some types of MPPT algorithms commonly used. Furthermore, PV system topologies are reviewed and different types of inverter are explained in this chapter.

Chapter 3 explains the basics of gird connection of distributed generation systems. It introduces IEEE and IEC standards for grid connection of distributed generators. Control of grid connected inverter, which includes the details about the control loops that are required, PWM generation for the inverter and interconnection of inverter with the grid, is introduced in this chapter.

Chapter 4 presents the designing of photovoltaic system in Simulink. The system power ratings are chosen in accordance with the equipment available at UiT-Narvik. All the devices used in the PV system are presented in this chapter.

Chapter 5 presents the simulation results of the system designed in Chapter 4.

In Chapter 6, the setting up of model for code generation using the embedded coder support package for texas instruments is presented.

Chapter 7 discusses the details and issues that were faced during the design process. It also provides the conclusion of this thesis work and recommendations for future work.

Introduction

2 PV System: A Review

This chapter provides detail about the building blocks of a photovoltaic system. It reviews different topologies that a system can be arranged in.



Figure 2.1: General Block Diagram of a PV System

2.1 Structure of PV System

Depending on the structure and configuration, PV systems are classified into four categories [7]. Fig 2.2 presents these four configurations. Each of them is briefly explained below.

2.1.1 Central Structure

In this system structure, individual PV panels/modules are connected in series to form what is called a string. This is done to achieve higher magnitude of DC voltage, which may directly be fed to the inverter. Then, multiple strings are then connected in parallel through string diodes to achieve higher current level. Central structure system has low efficiency because of losses in string diodes, mismatch between modules, a central MPPT for all the panels. They also require high voltage DC cables between the panels and the inverter [8].

2.1.2 String Structure

String structure of PV system is, in reality, a reduced form of central configuration, where only a single string of PV modules is connected to an inverter. There is no need of using string diodes and hence losses associated with them are removed. Losses associated with mismatch of modules

and partial shading are reduced as each string has its own MPPT. This increases the overall efficiency of the system. String structure increases the reliability of PV system.

2.1.3 Multi-String Structure

This structure is an advancement of string structure. This configuration is generally employed for high power rating systems. Each string has its own MPPT and DC-DC converter, but there is only one inverter which is common to all the strings. This configuration has the advantages of both central and string structures as higher power ratings and increased efficiency can be achieved with this setup. Strings with different orientations can be integrated in the in the system [8].



Figure 2.2: Structure of PV system [9]

2.1.4 AC module

AC module is the integration of PV panel and inverter into one device. All the necessary function like amplification of voltage and MPPT are integrated in the module. As there is only one PV panel, mismatch losses do not exist. Increasing the capacity of PV system is much more expensive than other structures.

2.2 Power Processing Stages

A PV system can also be classified in terms of the power processing stages that it has. There can be two types of PV systems according to this classification [9].

2.2.1 Single Stage System

In a single stage system, shown in fig 2.3, the inverter stage performs all the tasks which include MPPT, control of grid current and voltage amplification, if needed. A drawback of this configuration is that the inverter must be designed to handle twice the nominal power [9].



Figure 2.3: Single Stage System [7]

2.2.2 Multi-Stage System

The most common configuration for a multistage system employs two power processing stages. One of these two stage is a DC-DC converter while the other is the inverter as shown in fig. 2.4. DC-DC inverter handles MPPT in this scenario. In two stage system, either the output of the DC-DC converter is a DC voltage or the output current is modulated to follow a rectified sine wave [9]. In the case where output is a DC voltage, the converter is designed to handle just the nominal power and the inverter uses Pulse Width Modulation to control grid current. Whereas, in the other case, converter must handle twice the nominal power and also control the grid current,

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while the inverter switches at line frequency and converts the rectified sine wave current to a full sine wave.



Figure 2.4: Two-Stage System [7]

2.3 Power Decoupling

Power decoupling in a PV system is usually achieved by using a capacitor. In case of a single stage system, decoupling capacitor is placed between the inverter and PV panels. For a multistage system, it is paced between the output of DC-DC converter and inverter input. The value of decoupling capacitor can be calculated by using the equation provided in [9],

$$C = \frac{P_{PV}}{2 \omega U_C u} \tag{2.1}$$

where,

 P_{PV} is the nominal power of PV modules,

 ω is the rotational frequency of the generated sine wave,

 U_c is the mean voltage across the capacitor,

u is the amplitude of voltage ripple.

Decoupling capacitor is used to reduce the oscillatory nature of power obtained from PV modules [12]. This capacitor is usually an electrolytic capacitor and it is one of the main limiting factors in the life of a PV system. Electrolytic capacitors have a lifetime of 1000–7000 h at 105 °C operating temperature [10]. Figures 2.5 and 2.6 show the placement of power decoupling capacitor for a single stage and multi-stage system structure respectively.



Figure 2.5: Capacitor location in a single stage configuration [9]



Figure 2.6: Capacitor placement in Multi-Stage system [9]

2.4 Maximum Power Point Tracking

The power output obtained from a PV panel does not remain constant during the day. As the irradiance or temperature changes, so does the output power. Typical I-V curves with variations in irradiance levels and cell temperature are shown in fig. 2.7 and 2.8 respectively.





Figure 2.8: I-V curve with variation in Cell Temperature

It can be interpreted from the figures above that changes in irradiation and temperature leads to changes in power levels and there is only one point for a particular irradiance and temperature

level [13], where the power is maximum. To track this maximum power point, several algorithms are used, the most common of these MPPT algorithms are explained below.

2.4.1 Constant Voltage Algorithm

This method assumes that the maximum power point voltage is around 0.7 to 0.8 times the open circuit voltage of a PV panel/array. It also assumes that for changes in irradiance, the MPP voltage remains, more or less, constant and is only affected by changes in cell temperature [15]. Only one sensor is required the implementation of this algorithm.

2.4.2 Beta Method

This method relies on estimation of maximum power point through the equation mentioned in [13] which is dependent on electron charge, quality factor of junction panel, Boltzmann constant



Figure 2.9: Implementation of Beta method [13]

and number of cells in series in PV module or array. The value of beta remains almost constant at the optimum point with varying irradiance and temperature. So the value of beta is calculated using voltage and current of the panel/array and compared to a reference value in closed loop [15] control as shown in figure 2.9.

2.4.3 Perturb and Observe

This algorithm is based on perturbation of a control variable, which is either the output voltage of PV array, or duty cycle of the DC-DC converter switch(es). For the first case, a perturbation is applied to output voltage of PV array and a PI controller, consequently, adjusts the duty ratio of the converter. Tuning of PI controller in this case is done by using maximum power point value of PV array voltage [14]. In the case of direct duty cycle control, as the name suggests, a small perturbation is introduced in the duty ratio of DC-DC converter.

A major advantage of Perturb and Observe algorithm is that it is simple and easy to implement. Flowchart of direct duty ratio control P and O algorithm is shown in the figure 2.10



Figure 2.10: Flow chart of P and O [13]

2.4.4 Incremental Conductance

In this algorithm, the power (product of voltage and current) of PV array is differentiated w.r.t the PV array voltage and set equal to zero, and based on the value of the differential, the actual operating point is found. In this algorithm, unlike perturb and observe, PV array power doesn't have to computed. This algorithm provides very good transient performance i.e., when atmospheric conditions are changing. Flowchart of Incremental Conductance is shown in figure 2.11.



Figure 2.11: Flowchart of Incremental Inductance [13]

2.5 Inverter in a PV system

Inverters used nowadays in a PV system are self-commutated. The switching devices used in them can be power BJTs, IGBTs or MOSFETs, depending on the switching frequency and power density of the system. The inverters can be broadly classified into two types which are current source inverters and voltage source inverters. They are briefly explained below.

2.5.1 Current Source Inverter(CSI)

In a current source inverter, the input side (DC side) is a current source. The polarity of input current does not change and the direction of flow of power is determined by the input voltage. CSIs generate an alternating current wave at the output which has a fixed magnitude (for a given input) and adjustable time period. An inductor is connected at the input side of CSIs to maintain the current [7].

2.5.2 Voltage Source Inverter(VSI)

The input side of a voltage source inverter is a voltage source; a large capacitor is used for this purpose. The polarity of input voltage does not change and therefore direction of power flow is determined by the DC current input. Contrary to CSIs, alternating voltage of constant amplitude but variable can be obtained by using VSIs. Another feature of VSIs is that, they can be operated in both voltage control mode and current control mode.

Table 2.1 summarizes the differences between VSIs and CSIs. Table 2.2 provides the differences between voltage control and current control mode of VSIs.

Parameter	VSI	CSI
I/P Parameter	Voltage. Connected in parallel with a capacitor.	Current. Connected in series with an inductor.
Power Source	DC voltage source with negligible impedance.	The input of a CSI is changeable current from a DC voltage source having high impedance.

Table 2.1: Differences between VSI and CSI [16]

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Load Dependency	Voltage amplitude does not depend on load. O/P current waveform depends on load	Current amplitude does not depend on load. O/P voltage waveform depends on load
Associated Loss	High switching loss but low conduction loss. Thus total power loss is low.	Low switching loss but high conduction loss. Thus, the total power loss is high.

Table 2.2: Voltage and Current Control Mode of Operation [7]

Parameter	Voltage Control Mode	Current Control Mode
Inverter type	Voltage Source Converter (Self Commutated)	
Control Parameter	AC Voltage	AC Current
Fault S.C. Current	High	Depends on nominal current

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3 Grid Connected PV system

This chapter introduces the grid connection standards. It provides an insight into the control of inverter and the steps necessary to realize grid connection of photovoltaic systems.

Distributed generation systems can be broadly classified into two categories which are standalone and grid connected. In standalone systems, storage batteries are used which store the energy obtained from these intermittent sources. These batteries serve as input to the inverter, which converts DC power into AC power.

In grid connected systems, energy storage devices may not be used, as the energy obtained from light, in case of a PV system, can be directly converted to AC and transferred to the grid. To achieve this, the inverter must be controlled in a pre-defined way using control loops so that maximum power can be transferred to the grid. Also, the inverter's output terminals cannot directly be connected to the grid because of the harmonics that are present in current due to the switching nature of the inverter. A filter is used to negate this affect.

To connect a distributed generation system to the grid, there are several standards that are released by IEEE, IEC, NEC and EN (used in Europe) to guarantee safe interconnection and operation of the system and to maintain the power quality of the utility grid. First, the most relevant standards are presented and then the control structure of the inverter which includes grid synchronization, control loops and PWM generation, and filters that are used for a grid connected PV system are considered.

3.1 Standards for Grid Connection of PV systems

The most relevant standards for grid interconnection of photovoltaic systems are presented in this section. A brief introduction is provided to standards IEC 61727, IEEE 1547–2003 and IEEE 929–2000. Table 3.1 presents the parameters of these standards.

IEC 61727 [17] focuses on grid connected photovoltaic (PV) power systems which operate in with the utility and use semiconductor based inverters for DC to AC conversion. It provides specific recommendations for systems rated at 10 kVA or less, which may be used at individual residences, which may be single or tree phase. This standard applies to connection with the low-voltage utility distribution system.

IEEE 1547–2003 [18] provides guidelines for interconnection of distributed resources with electric power systems. It provides requirements relevant to the performance, operation, testing, safety considerations, and maintenance of the interconnection.

IEEE 929–2000 [19] contains recommended practice guidance regarding equipment/devices and functions necessary to ensure compatible operation of photovoltaic (PV) systems connected in parallel with the electric utility. This includes factors relating to personnel safety, equipment protection, power quality, and utility system operation.

Issue/Parameter	IEC 61727	IEC 1547	IEEE 929
Formation	U.K.	USA	USA
Nominal Power	10 kW or smaller PV	This standard covers	It contains sufficient
	systems	distributed	requirements for PV
	connected to low voltage	resources as large 10	systems of 10 kW or
	utility grid	MVA.	less. It also contains
			reasonable guidelines
			for larger systems up
			to
			500 kW.
Harmonic	(3-9) 4.0%	< 4% for (2–10) th	(3-9) 4.0%
currents(Order-	(11–15) 2.0%	< 2% for (11-16) th	(11-15) 2.0%
h)	(17–21) 1.5%	< 1.5% for (17–22) th	(17-21) 1.5%
limits	(23-33) 0.6%	< 0.6% for (23-34) th	(23-33) 0.6%
DC current	Less than 1.0% of rated	Less than 0.5% of the	The PV system
injection	output current	full rated output	should not inject DC
		current	current $> 0.5\%$ of the
			rated
			inverter output
			current into the AC
			interface under either
			normal
			or abnormal
			operating conditions
Voltage range	85–110% (196–253 V)	-	88–110% of nominal
for			voltage. Inverter
normal			should sense
operation			abnormal
	50 - 4 11		voltage and respond.
Frequency	50 ± 1 Hz	-	59.3-60.5 Hz
range for			
norman			
operation			

Table 3.1: Comparison of standards [7]

3.2 Control Structure of Grid Connected Inverter

Control system of a grid connected inverter is responsible for managing the power injection into the grid, obtained from a distributed generator. Mostly, a control structure based on two cascaded loops is employed for this purpose. A number of combinations of cascaded loops can be used, which include, outer power and inner current loop [20] and outer voltage and inner power loop [21]. But the most widely used strategy as mentioned in [22] is the one which uses a slower outer dc-link voltage control loop and a faster inner current control loop.

Voltage control loop is responsible for balancing the power flow of the system. If there is more power available from the dc side, the controller present in this loop changes the reference current so that more ac power can be injected into the grid. The current loop deals with maintenance of power quality and reduction of harmonics present in the current, so that it can be injected into the grid.

The control system can be designed in one of the three reference frames which are natural reference frame, stationary reference frame and synchronous reference frame. In natural reference frame, there needs to be a controller for each phase current. As the currents are sinusoidal non-linear controllers like dead beat and hysteresis are used in natural reference frame. Fig. 3.1 shows control structure in natural reference frame.



Figure 3.1: Control Structure in NRF [22]

In stationary reference frame control implementation, abc variable are transformed into $a\beta$ axis variables. Variables is this case are also sinusoidal. Proportional-Resonant controllers are normally used in stationary reference frame structure as PI controllers cannot remove steady state error in case of sinusoidal signals [22]. One possible implementation of control structure in stationary reference frame is depicted in fig. 3.2.



Figure 3.2: General Structure for Implementation of Control in Stationary Reference Frame [22]

In Synchronous reference frame, the sinusoidal variables are transformed into a frame that rotates at synchronous speed with sinusoidal variables, which makes these quantities appear as DC values. This means that PI controllers can be used as they provide satisfactory results when dealing with DC quantities [22]. Fig. 3.3 shows general control structure in SRF



Figure 3.3: General Control Structure in SRF [22]

As seen in figures 3.3 and 3.4, the cross coupling terms and voltage is fed forward in the control loop so that active and reactive power injection into the grid can be independently controlled [23]. SRF control structure is most commonly used.



Figure 3.4: Current Control Loop; Cross coupling [23]

3.3 Grid Synchronization

To achieve power flow between the renewable resource generator and the utility network, the injected current needs to be synchronized with the grid voltage. Different algorithms are used for grid synchronization. The main purpose of these algorithms is to obtain the phase information of grid voltages. Transformation from natural reference frame to stationary or synchronous reference frame may be required to make this possible [22]. Zero crossing method, Filtering of grid voltages and PLL are the methods that are used for grid synchronization. Among these three, PLL is the most widely used method. A brief explanation of PLL is presented below.

3.3.1 Phase Locked Loop (PLL)

PLL provides good rejection of harmonics and other disturbances. It is implemented in synchronous reference frame [24]. Fig. 3.5 shows the basic structure of PLL (a filter may be added to this so that negative sequence may be filtered out so that better performance can be achieved during asymmetrical grid faults). The phase lock is achieved by setting the reference d axis

voltage U_d^* to zero. A PI regulator is usually used to control U_d and the output of the controller is the grid frequency, which can be integrated to find the grid voltage phase angle [22].



3.4 Modulation Techniques for Inverter

To convert the DC voltage into an AC signal, the switches, present in an inverter, need to be switched on and off by providing pulses at their gates. There are a number of techniques that can be used to generate these pulses the most common being Space Vector based Pulse Width Modulation and Sine Pulse Width Modulation. As SPWM is used ought to be used in this work, it is therefore introduced here.

3.4.1 SPWM

In Sine wave based PWM, as the name suggests, a sine wave is used to modulate the carrier wave to generate switching signals. Figures 3.6 and 3.7 show the implementation of SPWM for a three phase, 2-level inverter. The frequency of reference sine waves dictate the frequency of fundamental component of generated waves. The frequency of carrier wave (triangular wave in figures) is the switching frequency of the inverter. In case of a two-level full-bridge voltage source inverter, there are six switches in total, with 2 switches in each leg for each phase.





The pulses shown in figures above are applied to the switches which are connected to positive dc bus rail in each leg, and a complimentary signal is applied to the switch connected to negative dc rail. This ensures that only a maximum of one switch is on at a time in a leg so that the DC bus does not get shorted.
3.5 Filter as Grid Interface

Inverters, as being switching devices cannot be directly connected to the grid. This is because the inverter produces harmonics which degrades power quality. There are different standards in place [17], [18] and [19] which put a limitation on the harmonics that can be injected into the grid. A transformer may be used to connect the system to the grid [25]. The windings of the transformer serve as inductance which reduces the harmonics present in the current wave. Transformers are expensive and bulky which leads to the system being costly. Therefore, a transformer-less topology to connect inverter to the grid has come into existence, and that is by using a filter circuit as the interface. There are three types of passive filters that are generally used, they are L, LC and LCL. These filters are shown in figure 3.8.



Grid Connected PV System

This chapter presents the steps that are used for designing the system in Simulink.

The main goal of this thesis is to design a grid connected photovoltaic system that can be used in the renewable energy laboratory at UiT Campus Narvik. In this chapter, the modelling of the relevant system in Simulink is presented. The capacity of solar modules that are currently present in the laboratory is used as the starting point in designing of the system. The example available from Mathworks as "Detailed model of a 100 kW Grid Connected PV Array" is used as the base model [27]. As model based designing technique is to be used, the designed model would be simulated in simulink and once satisfactory results are obtained, the control structure designed here would be used in generating code for target hardware. For this, new models would have to be designed in Simulink environment but with the use of peripherals of the dsp controller to be used as input and output to the model. This would be done is chapter 6.

4.1 PV Array

There are three solar panels available in the laboratory, each with a maximum power of 200 Watt. PV array block available in Simulink is initialized as shown in figure 4.1.

Block Parameters: PV Array PV array (mask) (link)	×
Implements a PV array built of strings of PV modules connect Allows modeling of a variety of preset PV modules available fi Input 1 = Sun irradiance, in W/m2, and input 2 = Cell tempe	ted in parallel. Each string consists of modules connected in series. rom NREL System Advisor Model (Jan. 2014) as well as user-defined PV modu rature, in deg.C.
Parameters Advanced	
Array data	
Parallel strings 1	
Series-connected modules per string 3	
Module data	
Module: User-defined	•
Maximum Power (W) 200.02	Cells per module (Ncell) 72
Open circuit voltage Voc (V) 44.5	Short-circuit current Isc (A) 5.92
Voltage at maximum power point Vmp (V) 36.5	Current at maximum power point Imp (A) 5.48
Temperature coefficient of Voc (%/deg.C) -0.27269	Temperature coefficient of Isc (%/deg.C) 0.061745
<	× ×
	OK Cancel Help Apply

Figure 4.1: PV Array Description

The three panels are connected in series which gives total open circuit voltage V_{oc} = 133.5V and maximum power point voltage at 1000W/m² and 25°C, Vmpp = 109.5V. The I-V and P-V curves at different temperatures and at different irradiances are shown in figures 4.2 and 4.3 respectively.



Figure 4.2: Array at different temperatures and irradiance of 1000W/m²



Figure 4.3: Array at different irradiances and 25°C temperature

4.2 DC-DC Converter

Two stage topology is chosen for the photovoltaic system. DC-DC converter, which is a boost converter in this model, takes care of maximum point tracking. The use of 2 stage topology makes the system customizable, i.e., it can be converted to a multi-string system to increase the capacity of the system in the future, with each string having its own MPPT and DC-DC converter.

As a solar cell is a current source, a capacitor C_{PV} of 30uF, calculated using equation 4 [31], is connected in parallel to the output from PV array, so that it appears as a voltage source to the boost converter. Boost converter is shown is figure 4.4. Perturb and Observe algorithm is used for extracting power from the array. The code for P&O is available in the appendix B.

$$C_{PV} = \frac{D V_{PV}}{4 \Delta V_{PV} f_s^2 L_{boost}} = \frac{(0.8673)(109.5V)}{4(10V)(4000^2)(4.8mH)} = 30\mu F$$
(4)

All the values used in equation 4 are derived later in this chapter.





4.2.1 Calculation of Boost Inductor and DC link Capacitor

The system is designed to be interconnected with a $400V_{LL}$ (rms) grid. This means that the DC link voltage should be high enough to guarantee this AC output. DC link voltage is calculated using:

$$V_{DC\ Link} = \frac{2\sqrt{2} \cdot V_{LL}(rms)}{m_a \cdot \sqrt{3}} \tag{4.1}$$

Where,

 $V_{LL}(rms)$ is the rms value of the Line to Line voltage value of the grid = 400V

 m_a is the modulation index which is chosen to be 0.87

This gives,

$$V_{DC Link} = 750V$$

To calculate the boost inductor [29],

$$L_{boost} = \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{\Delta I_L \cdot f_S \cdot V_{OUT}}$$
(4.2)

Where,

 V_{IN} is the input voltage to the converter = 109.5V

 V_{OUT} is the desired output voltage = 750V

 f_S is the switching frequency of the switch in boost converter which is chosen to be 4 kHz

 ΔI_L is the ripple current which is estimated using (taken as 13% of total current),

$$\Delta I_L = 0.13 I_{OUT} \frac{V_{OUT}}{V_{IN}} \tag{4.3}$$

 I_{OUT} is the maximum current that the array can provide = 5.48 A

The calculated value of inductor for the boost converter is,

$$L_{boost} = 4.8 mH$$

The DC link capacitor can be estimated using eq. (2.1). The obtained value with desired ripple of 3% i.e., 25V is,

$$C_{DC LINK} = 100 \mu F$$

4.2.2 Duty Cycle of Converter Switch

The duty cycle of boost converter is calculated using the formula:

$$D = 1 - \frac{V_{PV}}{V_{DC \,Link}} \tag{4.4}$$

During the simulation, irradiance changes from 1000 to 250 W/m2 and temperature changes from 25 to 50°C.

The duty cycle of the boost converter is calculated for irradiance of 1000 W/m^2 and cell temperature of 25 °C. As seen from fig. 4.2 and 4.3, V_{PV} = 109.5V, which gives,

$$D_{109.5V} = 0.8540$$

When irradiance is 1000W/m2 and temperature is 50°C, the array voltage reduces to 99.5V, as seen from figure 4.2. This means that the duty cycle should be increased to achieve the desired DC link voltage. The calculated value of duty cycle using equation 4.4 is,

$$D_{99.5V} = 0.8673$$

And it can be observed that change in array voltage ΔV_{PV} = (109.5V-99.5V) = 10V.

Perturb and Observe algorithm is applied for MPPT using direct duty cycle control method. The algorithm can be found in appendix B. The algorithm directly perturbs the duty cycle and checks if the power and voltage of the array increase or decrease, if both power and voltage increase, the next perturbation is in the same direction, otherwise the direction of perturbation is changed.

4.3 DC-AC Converter

Three phase, two level inverter, as shown in figure below is going to be used in this project. The switching devices are MOSFETs, as high switching frequencies compared to IGBTs can be obtained with MOSFETs. The DC lick capacitor serves as input to the inverter.



Figure 4.5: Three Phase Inverter

4.3.1 Control Structure of the Inverter

The most crucial part, other than obtaining maximum power from the PV array, is the control of the inverter. From grid synchronization to power flow management and pulse width modulation of the inverter, is taken care by the control structure of the inverter. In the designed model, the control takes place in synchronous reference frame. Equations 4.5 and 4.6 are used to transform voltage and current quantities from natural frame to dq reference frame. The designed structure is explained in this section, starting with the procedure to obtain grid voltage phase information.

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin(\omega t) & \sin\left(\omega t - \frac{2\pi}{3}\right) & \sin\left(\omega t + \frac{2\pi}{3}\right) \\ \cos(\omega t) & \cos\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} \times \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}$$
(4.5)

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin(\omega t) & \sin\left(\omega t - \frac{2\pi}{3}\right) & \sin\left(\omega t + \frac{2\pi}{3}\right) \\ \cos(\omega t) & \cos\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} \times \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}$$
(4.6)

4.3.1.1 Grid Synchronization

Phase information of the grid is obtained by using phase locked loop. The structure of PLL in Simulink is shown in figure 4.6. The necessary phase information is obtained. The phase angle is used in dq transformation of both the voltage and current quantities.



4.3.1.2 Control Loops

There are two control loops used to balance the power flow on DC and AC side and to increase the power quality fed into the grid. The outer loop in a voltage loop and the inner loop in a current loop. Modelling of control loops is carried out using [37] and [38] in Appendix A.

The voltage loop is used to keep the DC link voltage constant. When the input power from the solar array changes due to variation in irradiance or temperature, the DC link voltage would also change because the power obtained from the array would not match the power delivered to the grid [23]. The function of voltage loop controller is to change the active power reference current so that power obtained from the solar array can be matched to the power delivered to the grid. Voltage loop controller is shown in fig. 4.7.

The current control loop, based on the active power current reference and reactive power current reference (taken as 0 in this model, as the system only supplies active power to the grid), provides the desired voltage reference signals. Equations 4.7 and 4.8 are used in designing the current loop [28]. Fig. 4.8 shows the current loop controller.



Figure 4.7: Contents of Voltage Controller

$$V_{d_Conv} = V_{d_mes} - \omega L i_q + \left(K_P + \frac{K_I}{s}\right) \left(i_{d\ (ref)} - i_d\right)$$

$$\tag{4.7}$$

$$V_{q_Conv} = V_{q_mes} + \omega Li_d + \left(K_P + \frac{K_I}{S}\right) \left(i_{q (ref)} - i_q\right)$$
(4.8)

Where,

 $V_{d_{des}}$ and $V_{q_{des}}$ are d-axis and q-axis desired voltage references.

 V_{d_mes} and V_{q_mes} are d-axis and q-axis measured voltages.

id and iq are d-axis and q-axis measured currents.

 $i_{d(ref)}$ is the reference current obtained from voltage control loop and $i_{q(ref)} = 0$. PWM Generation



Figure 4.8: Contents of Current Controller

4.3.1.3 PWM Generation

The desired voltage reference signals V_{d_des} and V_{q_des} , obtained from current controller are now used to generate pulses for the six switches present in the inverter using Sine Pulse Width Modulation. These desired voltage references are first transformed back to natural frame, i.e., three phase quantities using the phase angle obtained via PLL using equation 4.9. A triangular wave of 30 kHz is used as carrier wave. The desired voltage waveforms are compared with the carrier wave, as shown in figures 3.6 and 3.7 in section 3.4.1, to generate gate pulses for the MOSFET switches of the inverter.

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin(\omega t) & \cos(\omega t) \\ \sin\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t - \frac{2\pi}{3}\right) \\ \sin\left(\omega t + \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} \times \begin{bmatrix} v_d \\ v_q \end{bmatrix}$$
(4.9)

4.4 Grid

The grid is modelled as a three-phase voltage source with a Line to Line rms voltage of 400V. A 600W load is connected to the grid as shown in fig. 4.9.



4.5 Filter

LCL filter is used to interconnect inverter with the grid in this design. As an inverter is based on switching devices and gating signals in the form of pulses must be provided for the switches, the output current can contain significant harmonic disturbances with tend to reduce power quality.

The criteria for calculating the values of the components is presented below. All the calculations are carried out using per phase circuit [29].

The inverter side inductor is sized as,

$$L_i = \frac{V_{DC\ Link}}{16.f_S.\Delta I_L} \tag{4.10}$$

Where,

L_i is the inverter side inductor per phase,

 f_s is the switching frequency of the inverter = 30 kHz,

 $V_{DC Link} = 750 V,$

and ΔI_L is the ripple current of the inductor which is chosen to be 10% of the phase current and can be computed using (4.11).

$$\Delta I_L = 0.1 * \frac{\sqrt{2} P}{V_{ph(grid)}} \tag{4.11}$$

Where,

P is nominal power of the system per phase = 200W

 $V_{ph(grid)}$ is the single-phase voltage of grid = 230V

After substituting these values, it is found that,

 $L_i = 13 mH$

The grid side inductance is computed using,

$$L_g = 0.6 * L_i$$
 (4.12)

This gives,

$$L_g = 7.8 mH$$

To find capacitance, the formula given in [29] is used. The capacitance is taken as 5% of base capacitance and calculated using,

$$C_f = 0.05 * C_b = \frac{P}{\omega_{grid} \cdot V_{ph(grid)}^2}$$
 (4.13)

Where,

P is the single-phase power = 200W,

 ω_{grid} is the rotational frequency of grid = 314.2 rad/s,

 $V_{ph(grid)} = 230$ V.

The obtained per phase capacitance for the filter is,

$$C_f = 0.6 \mu F$$

Per [30], a damping resistor in series with the LCL filter capacitor should be added to increase the performance of the filter. It is obtained using,

$$R_d = \frac{1}{3\,\omega_0\,C_f} \tag{4.14}$$

 C_f is the filter capacitor,

 ω_0 is the resonance frequency of the LCL filter which can be obtained using,

$$f_0 = \frac{1}{2\pi} \sqrt{\frac{L_i + L_g}{L_i C_f L_g}}$$
(4.14)

This results in $f_0 = 2943$ Hz, and the value of damping resistor needed is 30 ohms per phase. However, in the simulation, a lower value is used.

4.6 Block Diagram of the System



Figure 4.10: Block Diagram of the Modelled System

4.7 Summary

A summary of the parameters that are used is provided in tables below.

Input Power (max)	600W
Boost Converter input voltage (V _{PV})	109.5V
Input Current (I _{PV})	5.48A
L _{boost}	4.8mH
C _{PV}	30uF
V _{DC Link}	750V
C _{DC Link}	100uF
D99.5V	0.8673
D _{109.5V}	0.8540

Table 4.1: PV Array and Boost Converter Parameters

Table 4.2: Other Parameters

System Frequency (f)	50Hz
Grid Voltage (L-L)rms	400V
Inverter Side Filter (L _i)	13mH
Grid Side Filter (Lg)	7.8mH
Filter Capacitor (C _f)	0.6uF
Current Controller gains (kp, ki)	(0.6, 20)
Voltage controller gains (kp,ki)	(7, 800)

5 Simulation Results and Discussion

In this chapter, the results obtained from the designed model are presented.

The model designed in previous chapter is simulated in Simulink environment. The simulation is run for 2.5s with a sampling time of 1 us. The input signals to the PV array are time varying irradiance and temperature which are depicted in figure 5.1.



5.1 Solar Array

With the input signal to PV array as shown in fig 5.1, the maximum available power, as can be seen from fig 4.2 and 4.3 (in section 4.1 <u>PV Array</u>), at standard conditions is 600W and voltage at MPP is around 109V. At 50°C and 1000W/m² irradiance, the maximum available power reduces to around 550W and MPP voltage of around 100V.

5.2 DC-DC Converter

The DC-DC converter boosts the voltage of PV array to the desired voltage of 750V and helps in the application of Perturb and Observe algorithm of MPPT. Fig 5.2 shows the power that is extracted from the array by the application of the algorithm and the output voltage of the array while tracking the maximum power point.



Figure 5.2: Output Power of Array and MPP Voltage (MPP Tracking)

Fig. 5.3 shows the varying duty cycle of the switch of the boost converter for extracting maximum power from the array. When the panel voltage decreases at $1000W/m^2$ and $50^{\circ}C$, the duty cycle increases to around 0.8670. The duty cycle of the boost converter drops to 0.64 when the maximum power available is 150W at 250W/m2 and 25°C. This is because duty cycle and array voltage have indirect relationship. With change in irradiance, the array voltage tries to decrease, which can lead to system being knocked off the maximum power point. Here the function of MPPT algorithm comes into action, which decreases the duty cycle of the converter so that the

system can track the maximum power point. The DC Link Voltage is held constant by the voltage control loop.



Figure 5.3: Duty Cycle of Boost Converter

5.3 DC-LINK

The DC Link voltage is controlled by the voltage controller so that the power available from the PV array is equal to the power delivered to the grid. The reference signal for the voltage controller and the resulting dc link voltage is shown is fig. 5.4. When the ambient conditions change, the actual DC-Link voltage also changes, but the voltage controller pulls it back to the desired value.



Figure 5.4: Reference Voltage and Actual DC Link Voltage

5.4 DC-AC Converter

The inverter takes the DC Link Voltage and inverts it into an AC signal. This AC signal is a twolevel signal. The line to line voltage swings between -VDC LINK to +VDC Link as shown in figure 5.5. The signal shown is in the form of pulses with varying widths according to the amplitude of the reference sine wave. The fundamental frequency of this signal equals the grid frequency, which is 50 Hz.

5.4.1 Modulation Index

The modulation index of the inverter is shown in fig. 5.6. The DC Link voltage was chosen such that the inverter operates with a modulation index of 0.87.



Figure 5.5: Inverter Output Voltage Vab



Figure 5.6: Modulation Index of the Inverter

5.5 Three-Phase Voltage and Current Waveforms

After Synchronization of the inverter output with the grid, the inverter latches on to the grid voltages and the resulting 3-phase voltage waveform is shown in figure 5.7. The signals have a frequency of 50Hz and a magnitude of 230Vrms.



Figure 5.7: Three-Phase Voltage Waveform of Inverter/Grid

The three-phase current injected into the grid is shown in fig. 5.8. The magnitude of current of each phase is around 0.85 A (rms). The magnitude of harmonics present in the injected current w.r.t the magnitude of current at fundamental frequency for phase A and Total Harmonic Distortion of the injected current is shown in fig. 5.9. which is in reasonable limits.





5.6 Output Power

The power delivered to the grid is shown in figure 5.10. 581W are supplied to the grid when the available power from the PV array is 600W. When 552W power is available, 535W are fed into the grid. The overall efficiency of the simulated system is around 96%.



Figure 5.10: Power delivered to the Grid

5.7 Discussion About the Filter

The LCL filter that is required to reduce the harmonics present in the current, so that it is within limits set by the standards that are in place for grid connection of PV system, as calculated in chapter 4, has per phase inverter side inductance Li = 13mH, per phase grid side inductance Lg = 7.8mH and per phase capacitance Cf = 0.6uF. The values for the inductances are very high. The reason behind that is the fact that it is a 600W three phase system. This leads to per phase current being quite low which leads to the inverter side inductance Li, calculated using equation 4.10 and 4.11 to be 13mH. For a 1800W or a 3000W system, the inverter side inductances Li would be 4.3mH and 2.5mH respectively.

When the PV array size would increase in the on-campus laboratory eventually, the place where this designed system is intended for, the filter component value requirements would go down automatically. This is the reason behind continuing with system modelling for target hardware.

Simulation Results and Discussion

6 Model Designing for Code Generation

In this chapter, the setting up process of models for code generation is presented.

In model based designing process, system model has a central role. All the complexities and errors are taken care of in the designing of the model which took place in chapter 4. Now to continue the process, the control system designed in Simulink environment is used to generate code for target hardware which is a Texas Instruments C2000 Delfino F28335 DSP Controller [32].

Embedded Coder from Mathworks has a package called Embedded Coder Support Package for Texas Instruments C2000 Processors [33] that integrates a new library into Simulink, which contains the peripherals and sub-libraries of IQMath and digital motor control of the dsp controllers. These peripherals and sub-libraries are now used to make new hardware specific models based on the model designed in Chapter 4 so that code can be generated.

The control system is divided into two segments; hence two separate models are made. One is for the DC-DC converter control and the other for the inverter control as shown in fig. 6.1.



Figure 6.1: DC-DC Controller and Inverter Control

The DSP controller used, is in the form of a control Card [39] and a base board which is called peripheral explorer kit [40] is used to get all the necessary signals.

6.1 DC-DC Controller Model

The function of DC-DC controller is to sense the PV array voltage and current, apply the Perturb and Observe algorithm and generate PWM signal for the switch of the converter. The process to accomplish this and generate code is explained in this section.

6.1.1 **ADC**

The voltage sensor gives output of 3V for 115V input. The current sensor gives 3V output for a current of 10A. The outputs of voltage sensor and current sensor are connected to ADC A0 and A1 channels respectively. The ADC is of 12 bits in f28335 controller [35]. To get the actual value of signal, the value obtained is scaled first. The signal obtained from ADC needs to multiplied by the maximum voltage and divided by the total number of bits. The obtained value would be between 0-3V; this can be multiplied by the factor with which the sensor reduces the signal and actual signal magnitude can be obtained This action is summarized in equation (6.1).

$$Actual \ value = \frac{maximum \ ADC \ input \ level}{Total \ no. \ of \ steps \ of \ the \ digital \ output} \times \frac{maximum \ input \ of \ the \ sensor}{maximum \ output \ of \ the \ sensor} \ (6.1)$$

For the microcontroller used, maximum ADC input level is 3V and total no. of steps are 4096.

To start an ADC conversion event outside of a PWM event, the PWM block is initialized such that it triggers start of conversion for ADC after generating one cycle. The ADC block posts an

Block Parameters: Vpv, lpv C280x/C2833x ADC (mask) (link) Configures the ADC to output a constant stream of data collected from the ADC pins on the C280x/C2833x DSP.	×	Block Parameters: Vpv, Ipv × C280x/C2833x ADC (mask) (link) Configures the ADC to output a constant stream of data collected from the ADC pins on the C280x/C2833x DSP.
ADC Control Input Channels Module: A Conversion mode: Sequential Start of conversion: ePWMxA Sample time: -1 Data type: uint16 Post interrupt at the end of conversion	•	ADC Control Input Channels Number of conversions: 2 Conversion no. 1 ADCINA0 • Conversion no. 2 ADCINA1 • Use multiple output ports

Figure 6.2: ADC block configuration

interrupt after completion of conversion. The parameters of ADC block used in the design are shown in figure 6.2.

The sensed current and voltage of PV array is used in the MPPT algorithm, which generates the appropriate duty cycle.

6.1.2 **PWM**

The duty cycle obtained after application of MPPT, is converted to PWM signal using the PWM block available in the Embedded Coder Texas Instruments library. The time period of PWM [36] is calculated in clock cycles rather than seconds for better precision. The formula for calculating the clock cycles is given in eq. (6.2).

$$Clock \ Cycles = \frac{1}{2} \times \frac{f_{sys \ clk}}{f_{des \ PWM} \times TBCLK \times HSPCLKDIV}$$
(6.2)

Where,

TBCLK and HSPCLKDIV are prescalers, which are chosen as 1,

 f_{sysclk} is the clock frequency of the dsp controller = 150MHz,

 $f_{des PWM}$ is the frequency of the boost converter = 4kHz.

The above values result in 18750. But there is an offset, which was realized by testing the dsp controller, and can be balanced out by multiplying the clock cycles by 1.5. This results in,

Clock cycles =
$$28125$$

Channel PWM1A is used. End of PWM generation triggers the start of conversion for ADC. The configuration of PWM block is shown figure 6.3.

Block Parameters: ePWM X	Block Parameters: ePWM X	
C280x/C2833x ePWM (mask) (link)	C280x/C2833x ePWM (mask) (link)	
Configures the Event Manager of the C280x/C2833x DSP to generate ePWM w	Configures the Event Manager of the C280x/C2833x DSP to generate ePWM w	
General ePWMA ePWMB Deadband unit Event Trigger PWM	General ePWMA ePWMB Deadband unit Event Trigger PWM	
Allow use of 16 HRPWMs (for C28044) instead of 6 PWMs	Enable ePWM1A	
Module: ePWM1	CMPA units: Clock cycles	
Timer period units: Clock cycles	Specify CMPA via: Input port	
Specify timer period via: Specify via dialog	CMPA initial value:	
Timer period:	24131	
28125	Reload for compare A Register (SHDWAMODE): Counter equals to zero	
Reload for time base period register (PRDLD): Counter equals to zero	Action when counter=ZERO: Do nothing	
Counting mode: Up-Down	Action when counter=period (PRD): Set	
Synchronization action: Disable	Action when counter=CMPA on up-count (CAU): Clear	
Specify software synchronization via input port (SWFSYNC)	Action when counter=CMPA on down-count (CAD): Set Action when counter=CMPB on up-count (CBU): Do nothing	
Synchronization output (SYNCO): Disable		
Time base clock (TBCLK) prescaler divider: 1	Action when counter=CMPB on down-count (CBD); Do nothing	
High speed clock (HSPCLKDIV) prescaler divider: 1	Compare value reload condition: Load on counter equals to zero (CTR-Zero)	
	Add continuous coftware force input port	
	Continuous software force logici.	
	Continuous sortware force logic. Torcing usable	
	Reload condition for software force: Zero	
v	Enable high resolution PWM (HRPWM)	
Rinck Darameters: eDWM	×	
C280x/C2833x ePW/M (mack) (link)	() ()	
Configures the Event Manager of the C280x/C2833x DSP to generate ePWM way	veforms.	
Consul aDM/MA aDM/MD Deadhard with Event Trigger DM/M de	anna cashal Tria Zana unit	
Seneral ervivity ervivity Deadband unit Event myger Privity of	lopper control Trip zone unit	
Number of event for start of conversion for Medule A (SOCA) to be generated:	First quant	
Number of event for start of conversion for Module A (SOCA) to be generated:	inst event 👻	
Start of conversion for module A event selection: Counter equals to period (CTR	=PRD) 🔻	
Enable ADC start of conversion for module B		
Enable ePWM interrupt		
	OK Cancel Help Apply	

Figure 6.3: PWM block configuration

The designed model for DC-DC controller is shown in fig. 6.4 and 6.5.



f() function

Figure 6.4: DC-DC controller model



Figure 6.5: Contents of MPPT and PWM Generation Subsystem

When the solution is built, Simulink generates a .out extension file which can be programmed in the dsp controller using Code Composer Studio Integrated Development environment [34].

6.2 Inverter Controller Model

The code generated from this model is fed in DSP controller 2 of figure 6.1. The function of inverter controller is to read DC link voltage, three phase grid voltage and current injection into the grid, apply PLL, apply voltage and current control and generate PWM signals for the switches of the grid connected inverter. The design procedure is discussed briefly in this section.

6.2.1 ADC

Sensor for DC Link voltage gives 3V output for 800V input voltage. The output of DC link voltage sensor is connected to ADC channel B pin B0. The ADC input channels on an f28335 dsp controller are unidirectional. This means only positive signal of up to 3V can be inputted through the ADC channels. Voltage sensors that are used to measure the phase voltages vary their output between 0 to 3V centered around 1.5V for +350V to -350V input. The current sensor gives 0-3V also centered around 1.5V at the output for +/- 5A of current flowing through it. Vabc phase voltages are connected to ADC channel A pins A0, A1 and A2 and Iabc phase currents are connected to ADC A channel inputs A3, A4 and A5.

To get the actual positive and negative values of phase currents and phase voltages, equation (6.3) can be used.

Actual Value =
$$(ADC \ output - 2048) \times \frac{1.5}{2048} \times \frac{350V \ or \ 5A}{1.5}$$
 (6.3)

Start of conversion for ADC is triggered by PWM generation, as in DC-DC controller model, so that these two events don't overlap. ADC block configuration is shown in fig. 6.6 below.

Block Parameters: Va, Vb, Vcla, lb.lc-VDC(Link)	×	Block Parameters: Va, Vb, Vcla, Ib.Ic-VDC(Link)
C280x/C2833x ADC (mask) (link)	-	C280x/C2833x ADC (mask) (link)
Configures the ADC to output a constant stream of data collected from the ADC pins on the C280x/C2833x DSP.		Configures the ADC to output a constant stream of data collected from the ADC pins on the C280x/C2833x DSP.
ADC Control Input Channels		ADC Control Input Channels
Module: A and B	•	Number of conversions: 7
Conversion mode: Sequential	-	Conversion no. 1 ADCINA0 -
Start of conversion: ePWMxA	-	Conversion no. 2 ADCINA1 -
Sample time:		Conversion no. 3 ADCINA2 -
-1		Conversion no. 4 ADCINA3
Data type: uint16	-	Conversion no. 5 ADCINA4
Post interrupt at the end of conversion		Conversion no. 6 ADCINA5
		Conversion no. 7 ADCINB0
		Use multiple output ports
OK Cancel Help	Apply	OK Cancel Help Apply

Figure 6.6: ADC block configuration of Inverter Controller Model

Once the actual values are obtained, PLL is applied to get the grid voltage angle. This angle is used in abc-dq transformation and vice versa. The PLL block that was used in chapter 4 for Simulink model, among other blocks, cannot be used for code generation for hardware. Hence a Matlab function block is used which implements PLL. The code used for PLL can be found in appendix B. The voltage and current control loops designed in chapter 4 are replicated in this model.

After the desired reference signals are obtained in dq frame, they are transformed to three phase quantities and sent to ePWM blocks.

6.2.2 **PWM**

The desired abc reference signals are used for generating PWM signals for the switches of the inverter. The switching frequency was chosen as 30 kHz. This can be converted to clock cycles by using equation (6.2). After adding the offset, as discussed in DC-DC converter model, the clock cycles are found to be 3750. The three PWM blocks for phase A, B and C are PWM1A, PWM2A and PWM3A. These PWM blocks are configured appropriately to synchronize PWM generation for the three phases.

Model Designing and Code Generation

Figures below show how these PWM block are configured.

🔁 Block Parameters: ePWM 🛛 🗡	Block Parameters: ePWM X
C280x/C2833x ePWM (mask) (link)	C280x/C2833x ePWM (mask) (link)
Configures the Event Manager of the C280x/C2833x DSP to generate ePWM w	Configures the Event Manager of the C280x/C2833x DSP to generate ePWM w
General ePWMA ePWMB Deadband unit Event Trigger PWM	General ePWMA ePWMB Deadband unit Event Trigger PWM
Allow use of 16 HRPWMs (for C28044) instead of 6 PWMs	Enable ePWM1A
Module: ePWM1	CMPA units: Clock cycles
Timer period units: Clock cycles	Specify CMPA via: Input port
Specify timer period via: Specify via dialog	CMPA initial value:
Timer period:	2000
3750	Reload for compare A Register (SHDWAMODE): Counter equals to zero
Reload for time base period register (PRDLD): Counter equals to zero	Action when counter=ZERO: Do nothing
Counting mode: Up-Down	Action when counter=period (PRD): Do nothing
Synchronization action: Disable	Action when counter=CMPA on up-count (CAU): Clear
Specify software synchronization via input port (SWFSYNC)	Action when counter=CMPA on down-count (CAD): Set
Synchronization output (SYNCO): Disable	Action when counter=CMPB on up-count (CBU): Do nothing
Time base clock (TBCLK) prescaler divider: 1	Action when counter=CMPB on down-count (CBD): Do nothing
High speed clock (HSPCLKDIV) prescaler divider: 1	Compare value reload condition: Load on counter equals to zero (CTR=Zero)
	Add continuous software force input port
	Continuous software force logic: Forcing disable
	Reload condition for software force: Zero
< >	< >>
OK Cancel Help Apply	OK Cancel Help Apply

Figure 6.7: Phase A PWM block

Model Designing and Code Generation

Block Parameters: ePWM1 X	Block Parameters: ePWM1 ×
C280x/C2833x ePWM (mask) (link)	C280x/C2833x ePWM (mask) (link)
Configures the Event Manager of the C280x/C2833x DSP to generate ePWM waveforms.	Configures the Event Manager of the C280x/C2833x DSP to generate ePWM waveforms.
General ePWMA ePWMB Deadband unit Event Trigger PWM Allow use of 16 HRPWMs (for C28044) instead of 6 PWMs	General ePWMA ePWMB Deadband unit Event Trigger PWM
Module: ePWM2	CMPA units: Clock cycles
Timer period units: Clock cycles	Specify CMPA via: Input port
Specify timer period via: Specify via dialog	CMPA initial value:
Timer period:	2000
3750	Reload for compare A Register (SHDWAMODE): Counter equals to zero
Reload for time base period register (PRDLD): Counter equals to zero	Action when counter=ZERO: Do nothing
Counting mode: Up-Down	Action when counter=period (PRD): Do nothing
Synchronization action: Set counter to phase value specified via dialog	Action when counter=CMPA on up-count (CAU): Clear
Counting direction after phase synchronization: Count up after sync	Action when counter=CMPA on down-count (CAD): Set
Phase offset value (TBPHS):	Action when counter=CMPB on up-count (CBU): Do nothing
0	Action when counter-CMPR on down-count (CPD): Do nothing
Specify software synchronization via input port (SWFSYNC)	Action when counter-entry on down count (ebb). Do nothing
Synchronization output (SYNCO): Pass through (EPWMxSYNCI or SWESYNC)	Compare value reload condition: Load on counter equals to zero (CTR=Zero)
	Add continuous software force input port
Time base clock (TBCLK) prescaler divider: 1	Continuous software force logic: Forcing disable
High speed clock (HSPCLKDIV) prescaler divider: 1	Reload condition for software force: Zero
< · · · · · · · · · · · · · · · · · · ·	< >
OK Cancel Help Apply	OK Cancel Help Apply

Figure 6.8: Phase B PWM block

📓 Block Parameters: phase c 🛛 🕹	Block Parameters: phase c 🛛 🗙
C280x/C2833x ePWM (mask) (link)	C280x/C2833x ePWM (mask) (link)
Configures the Event Manager of the C280x/C2833x DSP to generate ePWM waveforms.	Configures the Event Manager of the C280x/C2833x DSP to generate ePWM waveforms.
General ePWMA ePWMB Deadband unit Event Trigger PWM	General ePWMA ePWMB Deadband unit Event Trigger PWM
Allow use of 16 HRPWMs (for C28044) instead of 6 PWMs	Enable ePWM3A
Module: ePWM3	CMPA units: Clock cycles
Timer period units: Clock cycles	Specify CMPA via: Input port
Specify timer period via: Specify via dialog	CMPA initial value:
Timer period:	2000
3750	Reload for compare A Register (SHDWAMODE): Counter equals to zero
Reload for time base period register (PRDLD): Counter equals to zero Counting mode: Up-Down	Action when counter=ZERO: Do nothing Action when counter=period (PRD): Do nothing
Synchronization action: Set counter to phase value specified via dialog	Action when counter=CMPA on up-count (CAU): Clear
Counting direction after phase synchronization: Count up after sync	Action when counter=CMPA on down-count (CAD): Set
Phase offset value (TBPHS):	Action when counter=CMPB on up-count (CBU): Do nothing
0	Action when counter=CMPB on down-count (CBD); Do nothing
Specify software synchronization via input port (SWFSYNC) Synchronization output (SYNCO): Disable Time base clock (TBCLK) prescaler divider: 1	Compare value reload condition: Load on counter equals to zero (CTR=Zero) Add continuous software force input port Continuous software force logic
High speed clock (HSPCLKDIV) prescaler divider: 1	Reload condition for software force: Zero
< OK Cancel Help Apply	< <u>OK</u> Cancel Help Apply

Figure 6.9: Phase C PWM block



Top level view of Inverter Controller model is shown in fig. 6.10.

Now, the solution for Inverter controller model can be built, as for the DC-DC controller model, and the controller can be programmed with the obtained file.
Model Designing and Code Generation

7 Discussion and Conclusion

This thesis work is based on designing a photovoltaic grid connected system for the power electronics laboratory of UiT-Narvik and using Embedded Coder feature of Simulink to generate code for this grid connected photovoltaic system. The code that would otherwise be handwritten, is generated by hardware specific model designed in Simulink environment. A summary about the procedure and discussion about issues that were faced during the design process are presented next.

7.1 Summary and Discussion

To accomplish the aforementioned task, using the model based design procedure, after reviewing the relevant literature, a Simulink model was designed. The solar array used for designing, has the specifications according to the solar modules present in the laboratory. Two stage topology, i.e., a DC-DC converter and inverter, was chosen for the system, as this would make enhancements in the future easy. The modules at the time of this thesis had a total capacity of 600W, and the array had maximum power point voltage of 109.5 V. Perturb and Observe technique was chosen for maximum power point technique because it gives reasonable tracking and it is simple to implement. The DC-DC converter used for the application of MPPT technique, had to also boost the incoming PV voltage quite significantly, as the DC link voltage had to be around 750V, because the grid Line to Line voltage is 400Vrms. This made the amplification that boost converter had to perform to be around 7 times. While this had no impact during the simulations, but it may lead to reduction in power output, because a boost converter normally has good efficiency for 5 times amplification, and the conduction losses might increase for higher amplification.

Two-level three-phase inverter was decided to be used, as it is simpler to design and implement. Phase Locked Loop technique was used for grid synchronization in the Simulink model. The control structure of the inverter was designed in synchronous reference frame as good performance in the voltage and current control can be achieved by using PI controllers.

The LCL filter required for filtering out the harmonics present in the current injected in the grid has an inverter side inductance of 13mH and grid side inductance of 7.8mH. These values are high because of the fact that the DC-Link voltage is very high and the power capacity of the system is only 600W, which make the per phase peak current very low, around 1.3A. As discussed in section 5.7, this results in the requirement of higher values of filter components to achieve the necessary filtering of harmonics. However, as the capacity of the system would increase, this issue would be resolved.

The next task was to use the designed model and use it for generating code that be used for programming the DSP controllers which were texas instruments delfino f28335 microcontrollers.

Two hardware specific Simulink models were made, one for the DC-DC Converter control and the other for grid connected inverter control, by replicating the control structure designed in the original Simulink model. There were some complications that were faced in the task. A number of Simulink blocks cannot be used for code generation. This includes the PLL block and transformation blocks, among others. Because of this PLL was implemented by writing code for it in Matlab function block. Data type problem was the other thing that took a lot of time to sort out. Finally, after the removal of errors, code was generated by using Simulink embedded coder.

Unfortunately, due to lack of time and limited resources, particularly, the unavailability of hardware (except the dsp controller and peripheral explorer board), the generated code count not be tested. Also there were some assumptions made regarding the sensors (in ADC scaling) used for obtaining inputs via ADC channels.

7.2 Conclusion

The task of designing a three-phase grid connected photovoltaic system and exploiting Simulink as a code generator has been successfully carried out in this thesis. The designed system is a single string system with two power processing stages namely, the DC-DC converter and DC-AC converter. Perturb and Observe MPPT algorithm is used for tracking of maximum power point, so that the system can be operated at maximum ratings for a given environmental condition. The control structure of the inverter is based on two loops, of which the outer loop is the dc link voltage control loop and the inner loop is the current control loop. An LCL filter is used for the interconnection of the inverter output with the grid. This filter provides the necessary filtering of harmonics present in the current because of the switching nature of the power electronic inverter. The simulation results are then studied and on achieving the desired results, the control structure of this Simulink model is used for code generation using the embedded coder support package for Texas Instruments devices. The Embedded Coder's Texas Instruments support package, which is used in this code generation procedure is still in its early phases and it can be observed that the associated library is more oriented towards motor control applications.

7.3 Recommendations for Future Work

Hardware testing of the generated code and differences in optimization level with hard-written code can be compared. Another enhancement could be designing of a multistring system. In this thesis, a 2-level inverter is used, systems using multilevel inverter and modular multilevel inverter could also be designed. This would be beneficial from an educational point of view as a lot of research is going on modular multilevel inverters and students can also become familiar with using Simulink as a code generator.

Discussion and Conclusion

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Appendix A: Current and Voltage Loops

Mathematical modelling

In this section, the controller gains for current and voltage control loop are calculated based of the transfer functions of the loops. Table 1 shows the base values that are used in the system. Table 2 shows the actual values and Per-Unit values of the components.

Base Voltage ($V_b = \sqrt{2} V_{ph rms}$)	325 V
Base Current ($I_b = \sqrt{2} P_{1ph} / V_{ph rms}$)	1.23 A
Base Impedance $(Z_b = V_b/I_b)$	264.22 Ω
Base angular velocity ($\omega = 2 \text{ pi f}$)	314.2 rad/s
Base Inductance(L _b)	0.84 H
Base Capacitance (C _b)	12 µF

Parameter	Actual Value	Per Unit Value
Converter side filter	13 mH	$L_{in pu} = 0.0155$
inductance (Li)		
Converter side filter	0.01 Ω	$R_{f pu} = 37\mu$
resistance (Ri)		
DC Link Capacitor(Cdc)	100 µF	C _{dc pu} = 8.33

Current Control Loop

The current loop is the internal loop. First the transfer function of this loop is obtained including the PI controller, because it is used in the voltage loop controller estimation. The control system is designed in dq reference frame and the component values are in per unit. Figure below shows the current control loop of d-axis current. Q-axis current loop is also similar.



LCL filter

The simplified transfer function of LCL filter as derived in [38] is given below.

$$L(s) = \frac{1}{sL_i + R_i} \tag{A.1}$$

This simplified transfer function of LCL filter is obtained by feed forwarding the cross-coupling term ($\omega L_i i_{iq}$) in d axis and ($-\omega L_i i_{id}$) in q axis current control loop. Furthermore, grid voltage is also fed forward as shown in figure below.



Where e_q and e_d are the grid voltage d and q components respectively.

After converting the actual values into pu values, the transfer function becomes,

$$L_i(s) pu = \frac{1/R_{i pu}}{1 + sT_{i pu}}$$
(A.2)

Where,

$$T_{i\,pu} = \frac{L_{\,i\,pu}}{\omega_b \,R_{i\,pu}} = 1.33s \tag{A.3}$$

Inverter

The inverter is approximated as a first order delay where the delay time is equal to half the switching time period.

$$I(s) = \frac{1}{1 + sT_{inv}} \tag{A.4}$$

Where,

$$T_{inv} = \frac{0.5}{f_{sw}} = 16\mu s$$
 (A.6)

fs is the switching frequency of the inverter, which is 30kHz.

PI Controller

PI controller transfer function is

$$C(s) = K_p \left(\frac{1 + sT_{int}}{sT_{int}}\right) \tag{A.7}$$

Where Tint is the Integral time constant and Ki = Kp/Tint

Overall Transfer function

The transfer functions of PI Controller, LCL Filter and Inverter are then multiplied. The resulting closed loop transfer function of the current control loop is:

$$M(s) = \frac{K_p}{T_{int} T_{inv} R_i} \left(\frac{1}{s^2 + \frac{1}{T_{inv}} s + \frac{K_p}{T_{int} T_{inv} R_i}} \right)$$
(A.8)

Modulus Optimum technique is used for calculating the gains Kp and Ki. According to MO, the largest gain in the system equals the Integral time constant,

$$T_{int} = T_{i\,pu} = 1.33s$$
 (A.9)

And K_p can be calculated as,

$$K_p = \frac{T_{i \, pu} \, R_{i \, pu}}{2 \, T_{inv}} = 1.537 \tag{A.10}$$

And K_i,

$$K_i = \frac{K_p}{T_{int}} = 1.156$$
 (A.11)

Voltage Control loop

The voltage loop is responsible for maintain the DC Link voltage. Voltage control loop is shown in figure below. This loop generates the d-axis reference current as the system is only injecting active power in the grid with unity power factor.



The PI controller transfer function is the same as in eq. (A.7). The first order system approximation of the current loop transfer function is carried out as mentioned in [38], because Symmetrical Optimum technique will be used for estimating the gains of voltage control loop, which results in:

$$M(s) = \frac{1}{1 + s2T_{inv}}$$
(A.12)

The DC Link (capacitor) transfer function is,

$$DC(s) = \frac{1}{sC_{dc}} \equiv (Conv. to p. u values) = \frac{\omega_b}{sC_{dc pu}}$$
(A.13)

The closed loop transfer function of voltage control loop is,

$$N(s) = \frac{K_p(1 + sT_{int})\omega_b}{K_p(1 + sT_{int})\omega_b + sT_{int}(1 + s2T_{inv})sC_{dc\,pu}}$$
(A.14)

Using the SO criteria, the integral time constant can be estimated as,

$$T_{int} = \sigma^2 \, 2T_{inv} \tag{A.15}$$

Taking parameter sigma as 2,

$$T_{int} = 2^2 \ 2T_{inv} = 12e^{-3} \tag{A.16}$$

For k_p,

$$K_p = \frac{C_{dc\,pu}}{2\,(2T_{inv})\omega_b} = 414\tag{A.17}$$

And K_i can be computed as,

$$K_i = \frac{K_p}{T_{int}} = 34500 \tag{A.18}$$

The computed values of gains for the current and voltage controller were used but the response was not satisfactory. This could be because the approximations and assumption that are used have left to a degraded model. However, the gains of the voltage controller and current controller that were present in the base model (Simulink example), were tried and they turned out to be working very well. As a result, these gains were used, which was also advised by my supervisor, as main objective of the thesis was not mathematical modelling of the grid connected inverter, but to study about the code generation aspect of Simulink.

Appendix B: Codes

MPPT algorithm

The Matlab code that was used for implementation of perturb and observe MPPT algorithm is presented below.

function D = PandO(Param, V, I)

- % MPPT controller based on the Perturb & Observe algorithm.
- % D output = Duty cycle of the boost converter (value between 0 and 1)
- % V input = PV array terminal voltage (V)
- % I input = PV array current (A)
- % Param input:
- Dinit = Param(1); %Initial value for D output
- Dmax = Param(2); %Maximum value for D
- Dmin = Param(3); %Minimum value for D

deltaD = Param(4); %Increment value used to increase/decrease the duty cycle D

persistent Vold Pold Dold;

if isempty(Vold)

Vold=0;

Pold=0;

Dold=Dinit;

end

P= V*I;

if (P - Pold) > 0

if (V-Vold) >0

```
else
  D = Dold + deltaD;
  end
else
  if(V-Vold)>0
   D = Dold + deltaD;
  else
   D = Dold - deltaD;
  end
end
if D > Dmax || D < Dmin
  D=Dold;
end
Dold=D;
Vold=V;
Pold=P;
```

D = Dold - deltaD;

PLL Algorithm

The PLL code implemented in matlab function block used for code generation for DSP controller 2 is presented below.

function [Theta,w] = fcn(V_in,Tsw)
%Single phase PLL based on "Grid Connected Inverters for Photovoltaic and
%Wind Power Systems" by Teodorescu, Liserre and Rodríguez page 53
%Code written by Bjarte Hoff
%Parameters

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Kpd = 0.1; Kp = 0.5; Ki = 1; Kvco = 1; wc = 2*pi*50; offset = -pi/2;

```
persistent i_LF_old;
if isempty(i_LF_old)
    i_LF_old = 0;
end
persistent i_VCO_old;
if isempty(i_VCO_old)
    i_VCO_old = 0;
end
```

```
%%Phase detector (PD)
e_pd = Kpd*V_in*cos(i_VCO_old);
%%Loop filter (LF)
i_LF = i_LF_old + Tsw*e_pd;
%Limit frequency deviatin to +-10Hz, that is +-63rad/s
if i_LF > 63
    i_LF = 63;
end
if i_LF < -63
    i_LF = -63;
end</pre>
```

```
%Output voltage to VCO
```

```
v_LF = e_pd*Kp+Ki*i_LF;
```

```
%%Voltage-controlled oscillator (VCO)
w_mrk = v_LF*Kvco+wc;
angle = i_VCO_old + w_mrk*Tsw;
%Scale to 0-2pi
while angle > 2*pi
  angle = angle - 2*pi;
end
angle_out = angle + offset;
while angle_out > 2*pi
  angle_out = angle_out - 2*pi;
end
while angle_out < 0
  angle_out = angle_out + 2*pi;
end
%Set output
%V_out = cos(angle);
Theta = angle_out;
w = w_mrk;
%Store old values
i_LF_old = i_LF;
i_VCO_old = angle;
```