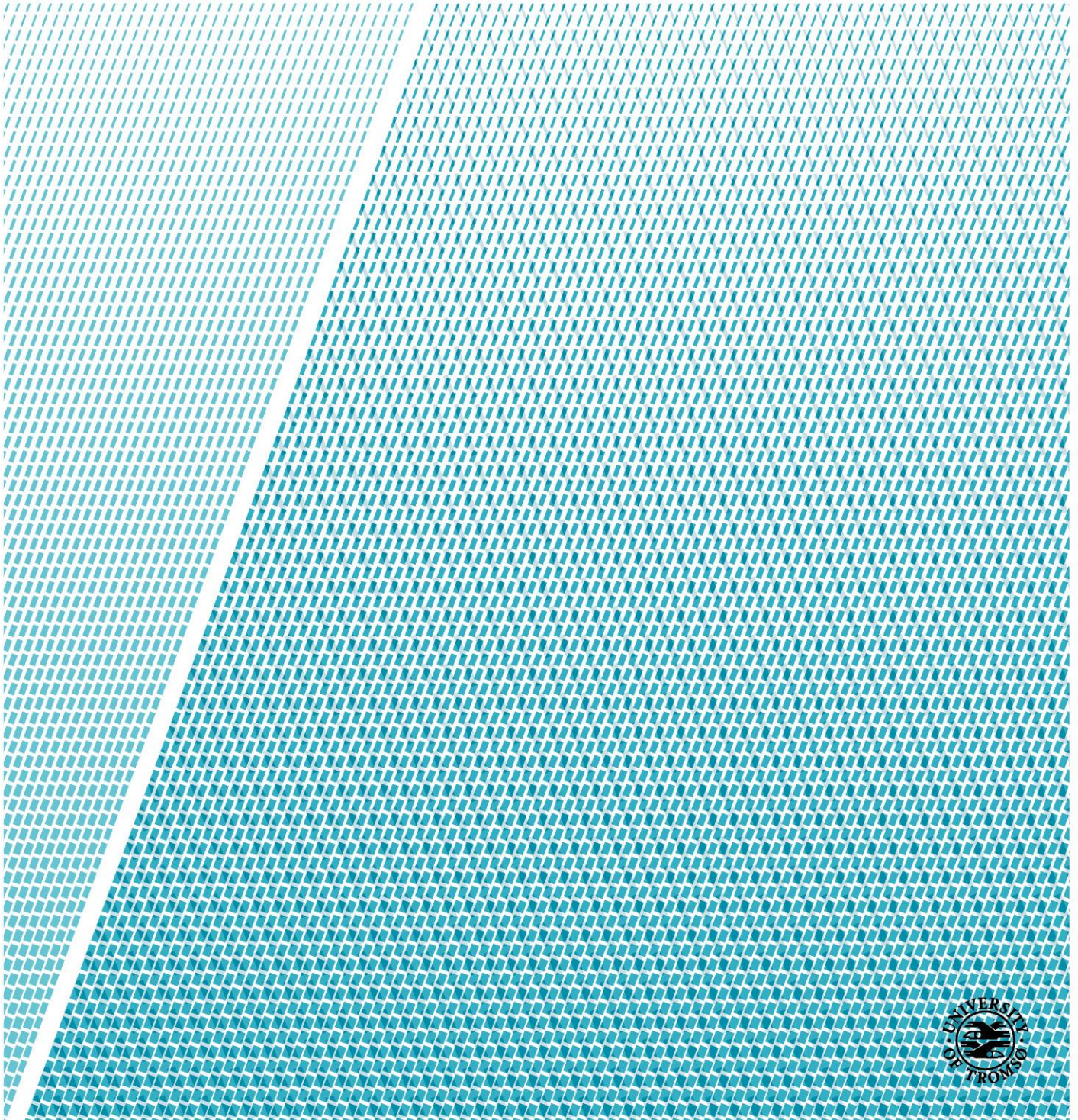


# Design and construction of a half-bridge using wide-bandgap transistors

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## **Abstract**

A continuously increasing demand of electric power makes energy efficiency imperative in modern technology. The transistor is considered as the fundamental element of modern electronic products.

Faster switching, lower losses and higher operation temperatures are some of the features provided by new transistor technology. Their abilities could make way for new converter topologies and design. It is also important to elaborate on the component limitations and to explore their traits. Therefore, thorough research regarding these transistors has been done.

This thesis goes through design improvements of a single transistor driver, both in form of simulations and experimental testing. Additionally, it discusses suggested solutions on how to build a snubber circuit, handle over current protection and apply dead time. Possible and preferred solutions for these parts are presented through circuit schemes and explanations. These parts should be put together in a half-bridge, as a building block for power converters. Other necessities, for the half-bridge, like control interface is briefly elaborated.

Required circuitry for implementing the single transistor driver, is designed and developed in OrCAD CAPTURE. Main experimental phases are evolving around this driver circuit for a wide-bandgap transistor. The single transistor driver is made as a simplified testing circuit for configuration in a half-bridge. The experimental circuitry has been constructed on a breadboard – using components, power sources and oscilloscope available at UiT Narvik. MATLAB has been used to present the results from the OrCAD CAPTURE simulation and oscilloscope from the experimental phase.

This thesis presents suggested schematics of a half-bridge building block for power converters.

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## Abbreviations

WBG	–	Wide-Bandgap
BJT	–	Bipolar Junction Transistor
FET	–	Field Effect Transistor
IGBT	–	Insulated Gate Bipolar Junction Transistor
JFET	–	Junction Field Effect Transistor
MOSFET	–	Metal Oxide Semiconductor Field Effect Transistor
V	–	Volt
A	–	Ampere
GaN	–	Gallium Nitride
SiC	–	Silicon Carbide
Si	–	Silicon
MMC	–	Modular Multilevel Converter
SSCB	–	Solid-State Circuit Breaker
CPLD	–	Complex Programmable Logic Device
OEM	–	Original Equipment Manufacturers
PV	–	Photovoltaic
EMI	–	Electro Magnetic Interference
PE	–	Power Electronics
IC	–	Integrated Circuit

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# 1 Introduction

As industrial products transition into more renewable solutions, the need for technological development is imperative. Wide-bandgap (WBG) devices, such as silicon carbide (SiC) and gallium nitride (GaN) can potentially operate at higher voltage and higher frequencies. Their switching losses is reduced by half[1], compared to older counterparts, meaning efficiency is increased. To exploit the WBG devices beneficial attributes, it is important to act with thrift considering design configurations.

Unique features provided by new WBG transistors secures development in electronic technology. With already enormous product possibilities, wide-bandgap material expands the horizon for transistor implementation. Consequently because of their ground-breaking characteristics, such as the performance during increased temperature[2]. Some products that already has implemented wide-bandgap technology features solar cells[3], microwaves [4] and several advanced energy efficient systems[5]. It is also expected that WBG devices will be featuring majorly in hybrid- and electrical vehicles by 2025 [1].

This thesis deals with the design considerations of a single transistor driver. The driver goals are to optimize switching time and oscillations, to utilize the transistor as efficiently as possible. This single transistor driver is a part of a whole system, creating a half-bridge module for power converters. Design developments are explored through simulation- and experimental results.

WBG power electronics are a less mature technology, compared to silicon (Si) counterparts, which means that there still are many unexplored possibilities of utilization.

## **2 Problem description**

### **2.1 Project assignment**

The following is stated in the project description:

*«In this project, a half-bridge should be designed as a building block for power converters based on wide-bandgap technology.»*

This implies that a solution should be produced for the half-bridge building block, with best possible specifications for the circuit and protection of the design. A control interface should also be created, while snubber circuits should be used to suppress voltage spikes. It is also stated in the project description that an optical fibre could be considered as medium, to increase safety and reduce noise in control signals.

Depending on time, a circuit board and mechanical layout could be created based on the design. The half-bridge should be used as a building block, making it possible to put together several half-bridges for different topologies. Experimental results should be produced from the half-bridge testing.

### **2.2 Project analysis**

The most demanding task of this thesis will be the design of the circuit. A main setup will be determined, making it possible to test several circuit solutions by only switching out or adding some components. The main setup also makes it achievable to easily compare transistors, thus highlighting the difference between normal transistors and WBG-transistors.

Simulation and testing of a half-bridge circuit could be done in several ways. An ideal simulation/experimental testing layout would have low aberration between each other. Consequently, a simple circuit configuration as possible is intended. Additional circuits for dead time and over current, should be tested separately or together with the final half-bridge circuit. This is because these circuits are not directly affecting the performance of the transistors in the half-bridge circuit.

## **2.3 Project limitations**

Design will be tested through simulation and prototype on a breadboard, but there will not be produced a finished design as part of the project. If there had been time for it, a printed circuit board would be ordered, instead of creating it manually. This also means that the optical fibre is not utilized as a medium. It could be interesting and educational to perform a soldering of a circuit, but it will provide for more efficient values during usage to order it. The finished product will not be used in a power converter before my thesis is delivered. Though, it could be interesting to see it used in a practical system.

## **2.4 Problem formulation/objective**

Can a half-bridge for power converters be designed using wide-bandgap transistors?

# 3 Wide-bandgap technology

## 3.1 Transistors

Transistors are used as switches in power electronic circuits. Their drive circuit is designed so that the transistor is either fully on or fully off. Transistors can be divided in to two main categories, the BJTs (Bipolar Junction Transistors) and the FETs (Field Effect Transistors), but there is also worth mentioning hybrid devices such as IGBTs (Insulated Gate Bipolar Junction Transistors). BJTs are current driven devices and they are characterized by less thermal stability, high noise levels and low input impedance. The FETs are classified as JFETs (Junction Field Effect Transistors) or MOSFETs (Metal Oxide Semiconductor Field Effect Transistors). They are voltage-controlled devices which has high input impedance, low noise levels, low power consumption and low heat dissipation as main attributes. While the FETs are unipolar, the BJTs are bipolar. This means that FETs either use only N-type or only P-type materials as main substrate. While BJT is built up by three layers of N-type- and P-type materials, structured either as NPN or PNP. The current flow from drain to source in a MOSFET is controlled by the gate to source voltage. [6]

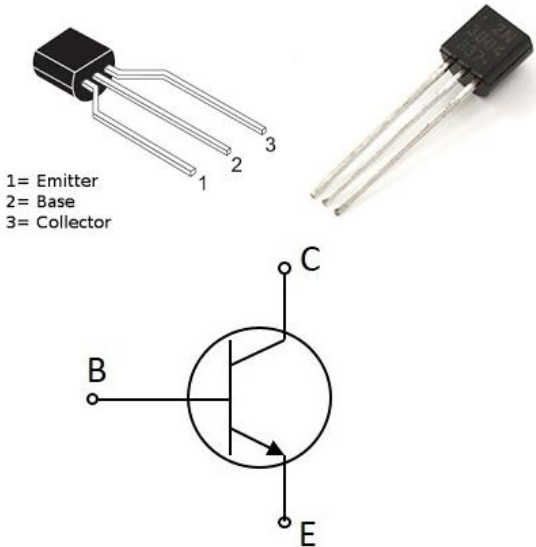


Figure 1 – Transistor: (Bipolar transistor structure - with collector, base and emitter) [7].

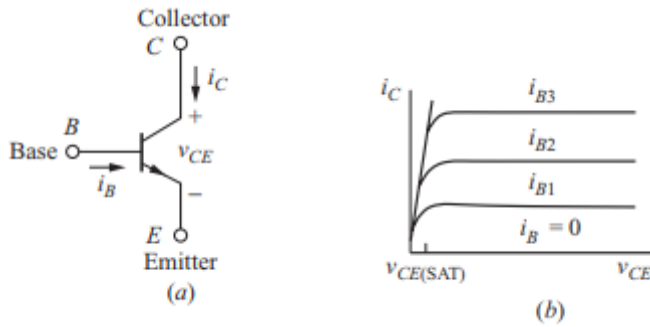


Figure 2 - BJT(NPN), with BJT characteristics[[8], p.9].

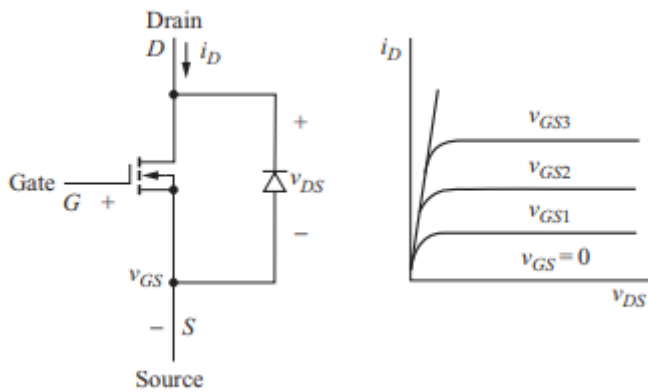


Figure 3 - MOSFET(N-type) with body diode, and MOSFET characteristics[[8], p. 9].

### 3.1.1 Limitations of normal transistors

There are limitations regarding normal transistors in electrical properties such as maximum:

- Switching speed.
- Gate voltage.
- Collector current/voltage (operating range).
- Gain.
- Thermal dissipation.

These limits are affected by the construction of the external circuit which the transistor is integrated in. They are also affected by the layout of the materials that forge the transistor (PNP/NPN/P-type/N-type). Maximum values should be mentioned in the transistor's datasheet, provided by the manufacturer.

### 3.2 Wide-bandgap transistors

There are endless opportunities in application of transistors. In recent years, there has been done much research on new transistor technology. Wide-bandgap (WBG) semiconductor devices allow faster switching operation, which results in lower switching losses. They can handle higher voltage levels and are also smaller in size, thus lighter in weight. Additionally, they have the possibility to operate in higher temperatures than normal transistors. This provides for the possibility of higher power values during normal circumstances. A WBG transistor is physically different in the crystalline level to materials such as silicon. It is identified as wide-bandgap if the bandgap is greater than 2 electron volts (eV) [9].

Silicon carbide (SiC) and gallium nitride (GaN) are the wide-bandgap materials that are most developed and up to date. They possess bandgaps of 3.3 eV and 3.4 eV respectively, compared to Silicon (Si) which has 1.14 eV bandgap [9].

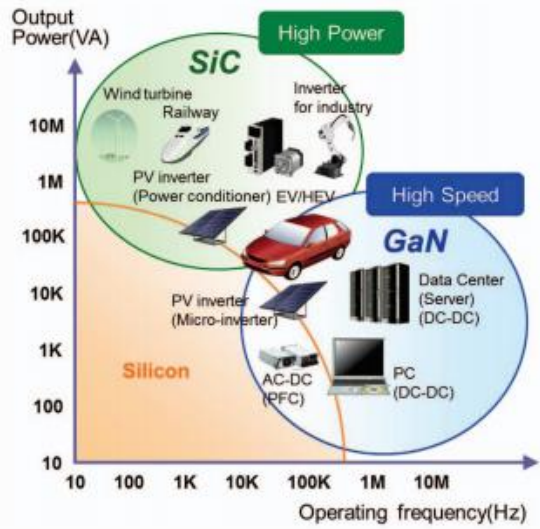


Figure 4 - Possible applications for SiC/GaN transistors

There has been done economic research on the WBG devices, like in 2016 it was posted a relevant SWOT analysis regarding these components [1].



<p><b><u>STRENGTHS</u></b></p> <ul style="list-style-type: none"> <li>• <b>WBG material properties lead to reduced energy use and system cost</b> <ul style="list-style-type: none"> <li>• Faster switching</li> <li>• Reduced losses</li> <li>• Increased power density</li> <li>• Higher operating temperature</li> </ul> </li> <li>• <b>Commercial SiC devices with required breakdown voltage for several applications available in US</b> <ul style="list-style-type: none"> <li>• SiC/GaN– 600V - 1.7kV</li> </ul> </li> </ul>	<p><b><u>WEAKNESSES</u></b></p> <ul style="list-style-type: none"> <li>• <b>Immature technology compared to Si</b> <ul style="list-style-type: none"> <li>• Higher cost</li> <li>• “Unproven reliability”</li> <li>• Low manufacturing level</li> <li>• “Design Inertia” <ul style="list-style-type: none"> <li>• Design for thermal benefits</li> <li>• Design for high frequency switching (EMI) <ul style="list-style-type: none"> <li>• OEM aversion to risk</li> </ul> </li> </ul> </li> </ul> </li> <li>• <b>Higher breakdown voltages and current capabilities are not available</b></li> </ul>
<p><b><u>OPPORTUNITIES</u></b></p> <ul style="list-style-type: none"> <li>• <b>Increase in energy needs</b> <ul style="list-style-type: none"> <li>• Increased desire to reduce energy use &amp; increase renewable energy generation</li> </ul> </li> <li>• Increasing government efficiency standards (global)</li> <li>• Government incentives for renewable energy generation</li> <li>• Growing supply chain <ul style="list-style-type: none"> <li>• Wafer &amp; discrete manufacturers</li> <li>• OEM WBG R&amp;D</li> </ul> </li> </ul>	<p><b><u>THREATS</u></b></p> <ul style="list-style-type: none"> <li>• Alternative energy savings techniques</li> <li>• Cost outweighing efficiency gains (e.g., PV inverters) <ul style="list-style-type: none"> <li>• Competition amongst U.S., Europe, China &amp; Japan may hurt global WBG market</li> </ul> </li> <li>• Adopting safety standards to include WBG PE</li> </ul>

Figure 5 - WBG integration SWOT matrix[1].

### 3.2.1 SiC power switches

SiC power switches are especially well suited for high temperature applications. That is because they can operate with very high thermal conductivity, compared to Si and GaN. It is the poly-type that is deciding the material properties of the transistor. SiC power switches can be both unipolar and bipolar. Unipolar meaning, there is two outputs (positive and negative (consider as ground)) where current flows from positive terminal to negative terminal. An example of a unipolar power switch is the SiC JFET, which is a good choice for voltage range between 1,2kV – 1,7 kV. This is because it has very low specific on-resistance as seen in Figure 6 – Si vs SiC structure [10]. The drift layer is 1/10 in SiC compared to Si. It can simultaneously operate at high- temperatures and frequencies.

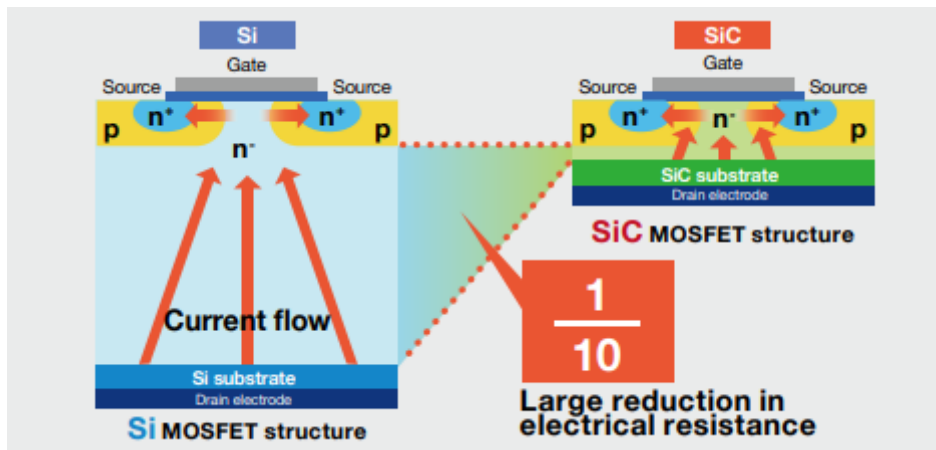


Figure 6 – Si vs SiC structure [10].

The bipolar power switch has three output terminals (positive, ground and negative), where negative terminal supplies an external circuit with electrons and the positive side pulls electrons from the external circuit. SiC IGBT is an example of a bipolar power switch, with cohering ability of blocking voltage capabilities over 10kV [11].

Different companies compete to provide the highest possible temperature operation on their transistors. For example, ST claim that they have the industry's highest junction temperature rating of 200 degrees Celsius on their portfolio of SiC MOSFETs. One of the key features of the SiC MOSFET is that it got higher breakdown voltage. That is approximately ten times more than silicon, and results in higher voltage capability [12]. SiC MOSFETs does not exhibit tail currents, like IGBTs does. Resulting in approximately 90% smaller turn off loss [13]. This allows the SiC MOSFET to switch at much higher frequency.

SiC-MOSFETs are relatively easy to drive and incur less gate drive loss because they are normally off voltage-controlled devices. IGBTs and Si-MOSFETs also have the same basic drive method as SiC-MOSFETs [13].

### 3.2.2 GaN power switches

Generally, GaN uses the AlGaN/GaN hetero structure, where two-dimensional electron gas (2DEG) is formed. Most GaN power switching transistors are formed on Si substrates, because of cost-reduction.

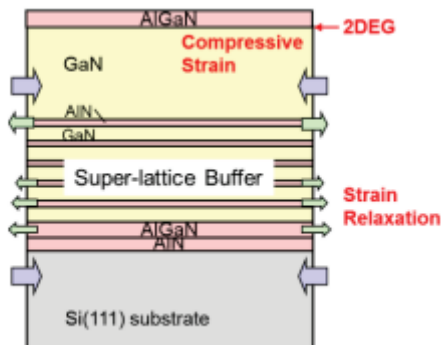


Figure 7 - AlGaN/GaN hetero structure on Si substrates [14].

GaN also offers some advantages over SiC and Si. As seen in Figure 8 - Material properties of Si, SiC and GaN [11], GaN possess the ability to utilize higher efficiency at higher switching frequencies. GaN switches is estimated to have ten times the performance advantage over SiC [15]. Mostly due to high breakdown field, but also high electron- mobility and velocity. The GaN switch does not need a freewheeling diode, eliminating costs and losses. GaN devices causes inconvenient parasitic ringing. Measures should be taken to prevent these noises. Manufacturers face the challenge of balancing large volume production at a competitive price while maintaining high performance and reliability compared to SiC counterparts. This is because a well-defined global epitaxial relationship between the epitaxial GaN film and the substrate is needed to grow a high-quality, single-crystalline GaN film [11].

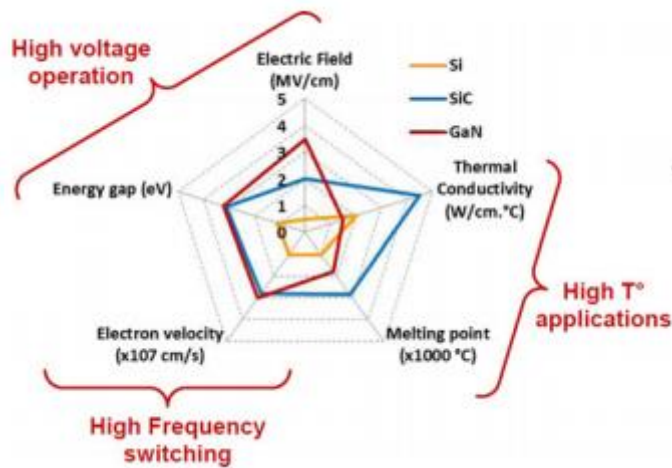


Figure 8 - Material properties of Si, SiC and GaN [11].

### 3.2.3 WBG limitations

Most of the companies that sell wide-bandgap semiconductors are not highlighting the challenges of these components. Their focus is on the technical progression and new usage areas of WBG transistors, compared to early and less developed types. Despite new high technological WBG-transistors, there are some disadvantages.

The SiC and GaN power transistors can cause electromagnetic interference (EMI) and leakage currents because of fast switching of currents ( $di/dt$ ) and voltages ( $dv/dt$ ) [16]. High  $di/dt$  and  $dv/dt$  can cause these events due to stray capacities. There are challenges with SiC and GaN because of their quick response time, which also creates noise/disturbance [14].

The most serious technical issue of the AlGaN/GaN structure applied in GaN transistors has been “current collapse”. This happens when the drain current is decreased after applying high drain voltages [17].

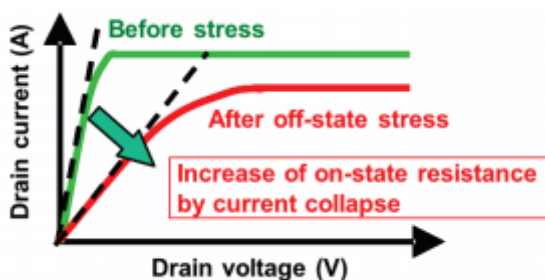


Figure 9 - Current collapse in GaN transistors [14].

In SiC DMOS it has been reliability issues when applying high positive or negative gate voltages, because trapped electrons was resulting in shift of the threshold voltages [14]. Another consideration is the body diode, because it has the same active material as the main MOSFET. The diodes conduction can lead to losses that heat up the MOSFET part, which over a longer period can affect the transistor reliability. The SiC body diode has an advantage in half-bridge configurations, because it is usually softer than the one in silicon, and that is reducing reverse recovery losses [18].

When handling high frequency SiC power devices, it is important to consider EMI. The fast switching of SiC MOSFETs can lead to an immoderate ringing noise. It occurs when the circuits switches turn on and off. The noise is caused by the high frequency resonance between the internal capacitance of the inductor and stray inductance in the switching power loop. To reduce the EMI – the required operation is to use a single layer winding inductor in the circuit [19].

When SiC MOSFETs operate in a phase-leg configuration a common problem is occurring. It is concerning the interaction between the two switching positions during the switching transients. The drain – gate capacitance of the SiC MOSFET (either the upper or the lower position) is forced to recharge. This can cause mistriggering of the other device connected in the phase-leg [20].

Looking at the economical aspect of this, Si are sometimes ten times cheaper than SiC counterparts. WBG power electronics are also less mature in technological development, which means that there could be concerns regarding the reliability of the components. This lack of maturity also leads to lower voltage handling, lower production volumes, and current handling capabilities [1].

SiC MOSFET and cascode GaN transistor were tested in a DC-DC boost converter, regarding noise [16]. The following paragraph is based this paper:

*The external gate resistor value in a DC-DC boost converter has almost no effect on the conducted noise spectrum level for the GaN transistor (contrary to the SiC MOSFET), in high frequency range (10 – 120 MHz). GaN transistors have high noise levels especially at turn-on operation. This is a consequence from the fast switching and large ringing oscillations in the gate voltage.*

*To fully exploit the performance of GaN transistors, it is required a gate drive circuit and package optimization for minimum parasitic inductance. Turn on speed and dynamic characteristics is factors that influence the EMI levels up to 100 MHz. This has been proved through experimental exercises with a DC-DC boost converter, where SiC MOSFET and cascode GaN transistors have been used. The GaN transistor enable faster transition of voltage and current [16].*

### 3.3 SCT3120AL

This wide-bandgap transistor is a N-channel silicon carbide power MOSFET, that features electrical ratings well inside the required criteria (drain-source voltage = 400 V and drain current = 16 A). It has a drain-source voltage at 650 V and drain current at 21 A (at 25°C) [21].

A simulation model of the WBG transistor is not yet available in pSPICE. Though, a spice model was available as a .lib-file from the manufacturer. A simulation model was created by adding this file to the library of the OrCAD Capture project. The same .lib-file should also be added to the simulation profile. This was done in the simulating settings, by adding it as a global in the configuration files menu. It was then possible to perform simulations with the SCT3120AL WBG transistor.

The switching time is defined by how fast it charges the gate terminal on and off.

The transistor datasheet determines its switching time capabilities. Simulations and physical tests will therefore be idealised towards these values.

Turn - on delay time	$t_{d(on)}^{*5}$	$V_{DD} = 300V, I_D = 6.7A$ $V_{GS} = 18V/0V$ $R_L = 45\Omega$ $R_G = 0\Omega$	-	14	-	ns
Rise time	$t_r^{*5}$		-	21	-	
Turn - off delay time	$t_{d(off)}^{*5}$		-	23	-	
Fall time	$t_f^{*5}$		-	14	-	

Figure 10 - Switching times from SCT3120AL datasheet.

# 4 Half-bridge

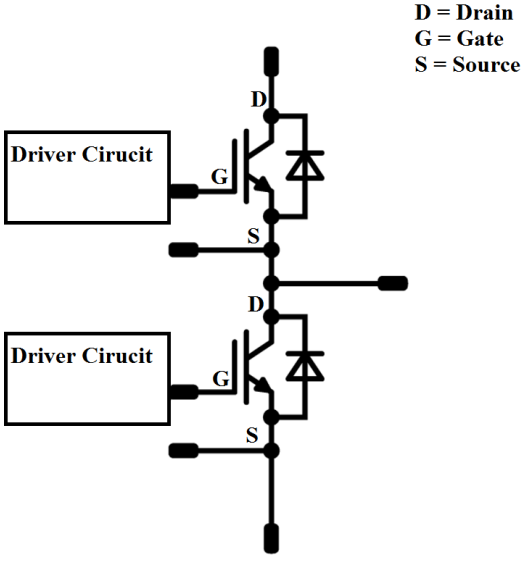


Figure 11 - Half-bridge module.

A half-bridge is built up by two similar transistors in series, as shown in Figure 11 - Half-bridge module. The transistors function as switches, and it is therefore desired that they can switch as fast as possible under any circumstances (ideally). The half-bridge requires a driver circuit on the base/gate of each transistor to control the power flow.

It is also imperative to implement circuit protection. Firstly, the switches should be opened and closed at the right time. This could sometimes create interference, meaning dead time must be implemented. If dead time is not included, it could mean that one transistor is turning on while the other one is still in the process of turning off.

Overcurrent protection should also be applied, to get rid of faults and preventing the circuit from being harmed. An important circuit addition which should be added to remove voltage- and current spikes, is a snubber circuit. This is constructed by a diode, resistor and capacitor in parallel and is placed physically as close as possible to the transistor. Other circuitry is dependent on application. This type of module can for example be used in motor drives, inverters and converters. Half-bridges are also very relevant for usage in renewable energy applications.



## 4.1 Half-bridge converter

A half-bridge converter is categorized as a DC-DC converter. It can supply an output voltage higher or lower than the input voltage and is isolated to forward topology. The half-bridge converters have typical power-ranges between 300 – 1000 W. Both high-side- and low side drivers are needed for half-bridge converters.

The following dots presents some of the advantages of a half-bridge converter.

- Voltage stress on switches is only input voltage.
- No ringing at switch node.
- Diodes are clamping leaking energy. Additionally, the leakage energy is recovered to input capacitors. Meaning there is low EMI and high efficiency.
- Suitable for a wide range of applications.

Half-bridge converters do not necessarily have disadvantages. Though, there are some concerns regarding the switches.

- Switches turn on/off -> nonlinear time-varying phenomena -> increased switching voltage and current ripples -> damage circuit elements [22].
- Switching power loss (Snubber circuit reduce these losses).
- Parasitic oscillation when MOSFETS are used as switches.

A half-bridge can also be used in inverter topology [23].

## 4.2 Half-bridge converter applications

There are many types of half-bridge converter configurations such as:

- Buck
- Boost
- Buck-Boost
- Cuk

Half-bridges have several application possibilities. If two half-bridges are put together they form a full-bridge [24].

Other usage options are three-phase connection or modular multilevel converter (MMC). In MMC, an ‘arm’ of half-bridge sub modules is created by connecting the modules in series. To

control the circulating currents and limit the fault currents, a reactor L is also added in the circuit [25].

**4.2.1 Half-bridge buck converter**

The main objective of this thesis is to design a half-bridge as a building block for power converters. To understand how a converter works, an analyse must be performed to see what happens during the different stages of the converter switches.

As it is observed from the circuitry between  $V_s$  and the primary side ( $N_p$ ) of the transformer in Figure 12 (a), there is a capacitor divider.

This means that there is a half of the input voltage available across the transformer winding.

The switches (Sw1 and Sw2) opens and closes in the given order shown by in Figure 12 (b). This sequence results in an alternating voltage pulse  $V_p$  on the transformers primary side. The maximum voltage stress over the switches is equal to  $V_s$ .

**4.2.1.1 Switching sequence analysis**

The following procedure describe the switching as in (b). Unipolar switching is applied.

Sw1 is closed – Sw2 is open:

A voltage  $\frac{1}{2} * V_s$  is present on the transformer primary side, forcing  $\frac{1}{2} * V_s * N_p / N_s$  (half of input voltage \* winding ratio) at the secondary winding ( $N_s$ ) of the transformer. It is forcing a magnetizing current across our rectifier

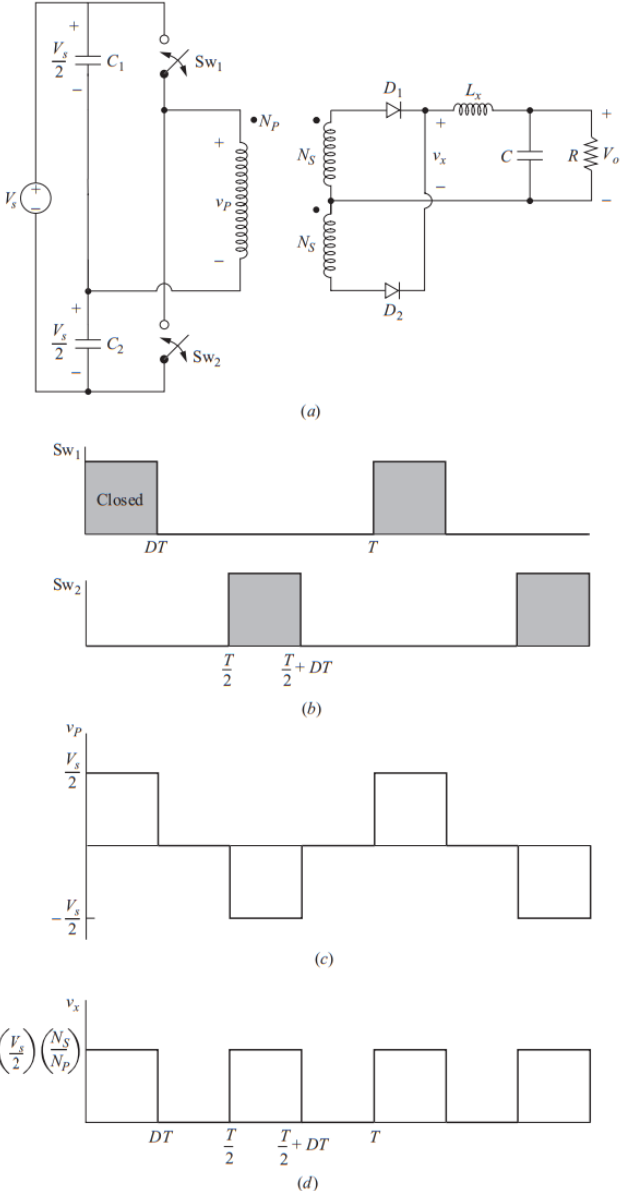


Figure 12 - (a) Half-bridge buck converter, (b) Switching sequence, (c) Voltage on the transformer primary, (d) Voltage Vx

D1 and our storage choke (Storage chokes task is to smooth the pulsating current, by storing energy during the ON duty cycle.).

*Open Sw1:*

The output voltage is present at L1 causing the freewheeling current. This current is separating and dividing 50 % by rectifier D1 and rectifier D2.

Next cycle starts by switching *Sw2 to closed (high side)*, and the procedure repeat itself the other way around.

The relationship between the input and the output of a half-bridge buck converter is given by:

$$V_o = V_s * \left( \frac{N_s}{N_p} \right) * D \quad (1)$$

D is the duty ratio of each switch.

# 5 Over current protection

Power semiconductor devices requires protection to avoid being damaged. Excessive voltage, current and certain rates of changes are the factors that can hurt the device. Fuses is not a sufficient solution, because they are not fast enough [[26], p.717].

Overcurrent protection of silicon carbide MOSFETs is challenging because the short circuit withstand time is very short. Some papers present methods to prevent over current and improve reliability. These methods present the ability to clear a short-circuit fault within 200 ns [27]. There has been reported that short circuit events over 80  $\mu$ s, can influence the reliability of the SiC MOSFET. This is because it can cause damage to the gate-oxide layer. To ensure long term stability, the overcurrent protection should be rather fast [20].

## 5.1 Desaturation technique

This method implements a sensing diode to detect the drain-source voltage when an overcurrent fault occurs [27].

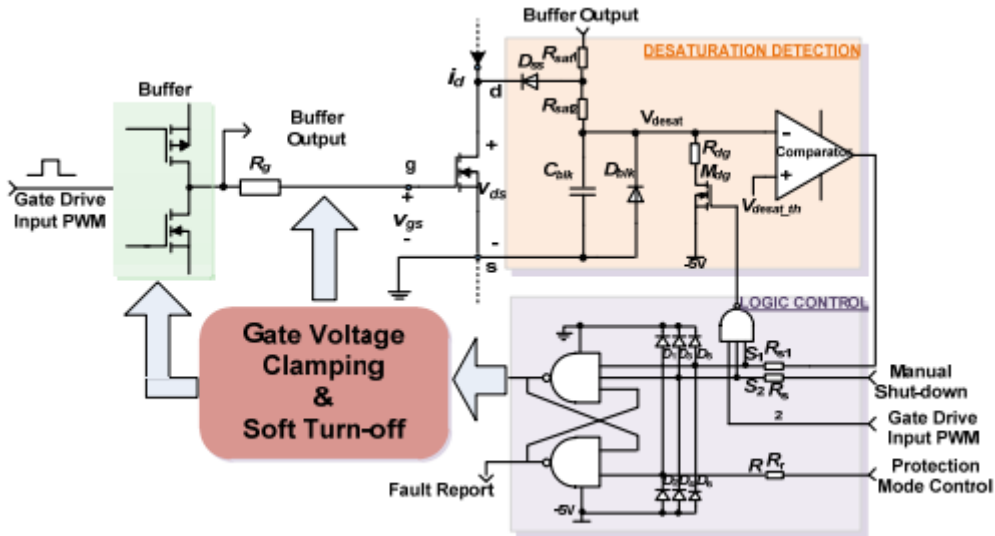


Figure 13 - Desaturation detection with logic control [27].

An advantage of this method is that it has a fast fault response time. A disadvantage could be that its performance is dependent on temperature. This technique is highly dependent on the characteristics of the SiC MOSFET.

## **5.2 SSCB**

Another possibility is to use a solid-state circuit breaker (SSCB). Mainly composed by a Si IGBT, but a commercial gate driver IC in series with the DC bus is also required to detect and prevent overcurrent faults. This method is independent of the SiC MOSFETs switching characteristics but can cause complicated main power circuit packaging. The SSCB is not affected by eventual large temperature changes but has slower fault response time than the desaturation technique [27].

## **5.3 Circuit breaker**

A circuit breaker is a component that can open when experiencing an excessive current. AC circuit breakers are often used in industrial solutions, and the required current to open the switch is usually much higher than the operating current. A high arc voltage should be generated at the breaker contact point to reduce the fault current in a DC circuit breaker [28]. A circuit breaker also has an input power disconnect switch. Unfortunately, a circuit breaker should not be used in this type of task. This is because the time it takes for the circuit breaker to disengage, is too slow to protect a transistor.

## 6 Dead time

Dead time is something that is implemented to avoid that upper and lower transistor is on simultaneously. Important considerations regarding high power and high frequency converter operations are evolving around increased losses and voltage waveform distortion. When dead time is active, the current runs in the freewheeling diode. If the delay time is quicker, the dead time requirements will also be quicker. This delay time can be minimized by creating the driver circuit correctly. It would be preferred an ideal delay time, to prevent unnecessary waste of energy.

As best-case conditions in a half-bridge configuration, one transistor has just turned off when the other transistor turns on. To achieve the necessary delay so this condition can be applied, is equal to the maximum value of the propagation delay difference specification (given as “Pdd” in datasheets). The propagation delay specification is also used to find maximum dead time. It is given as the difference between maximum and minimum Pdd [29].

There are several possible dead time configurations. It is possible to create a gate driver with a dead time controller [30]. Alternatively, one solution describes a logic adaptive dead time controller [31], though this is preferably constructed for GaN transistors. The solution presented for dead time in this thesis is an RCD delay circuit.

## 6.1 Delay time

To idealize the driver circuit, it is crucial to know what happens when a switch transient occurs. Analyses show the four phases of a switching transient, during turn-on [32].

1. Turn-on delay time [  $V_{negative}$ ,  $V_{threshold}$  ]
2. Rising drain current [  $V_{threshold}$ ,  $V_{plateau}$  ]
3. Falling drain source voltage [  $\cong V_{plateau}$  ] (Miller plateau voltage)
4. Changing on-resistance enhancement [  $V_{plateau}$ ,  $V_{positive}$  ]

The order of four phases of the switching transient is reversed during turn-off.

The turn-on delay is defined as the time from the gate starts to be charged until the drain current starts to rise, which is when the gate voltage reaches the threshold voltage,  $V_{threshold}$ . Similarly, the turn off delay is defined as the time from the gate starts to be discharged and until the drain-source voltage starts to increase.

Delay time increases with higher threshold values of resistance and capacitance. Note that turn-on delay becomes larger when applying negative driving and turn-off delay will be quicker when plateau voltage is increased.

$$t_{delay,on} = \ln \left( 1 - \left( \frac{V_{threshold} - V_{negative}}{V_{positive} - V_{negative}} \right) \right) * \tau \quad (2)$$

$$t_{delay,off} = \ln \left( 1 - \left( \frac{V_{positive} - V_{plateau}}{V_{positive} - V_{negative}} \right) \right) * \tau \quad (3)$$

$$\tau = R * C \quad (4)$$

$$R \cong R_{g,EXTERNAL} + R_{g,INTERNAL} + R_{driver,INTERNAL} \quad (5)$$

$$C \cong R_{gate,INPUT} \quad (6)$$

It is also worth mentioning that the gate current is in control of both  $di/dt$  and  $dv/dt$  [32]. This is observed through the second and third step of the switching transient. Because when the gate voltage is rising, and the device channel is opening, the drain current is changing. When this occurs, the gate current is charging the gate source capacitor. The change in drain current is controlled by the gate current. In the same way, the  $dv_{DS}/dt$  is controlled by the gate current when gate voltage is at the plateau voltage.

$$\left( \frac{di_{Drain}}{dt} \right) = gm * \left( \frac{dV_{GateSource}}{dt} \right) = gm * \left( \frac{ig}{C_{GateSource}} \right), V_{GateSource} \in V_{thermal}, V_{plateau} \quad (7)$$

$$\left( \frac{dv_{DrainSource}}{dt} \right) = \left( \frac{i_{Gate}}{C_{GateDrain}} \right) \quad (8)$$

Circuit implementation would be complicated, but necessary. Though, there is an alternative, and that is to apply a CPLD programmable device into the circuit. More on that in the next chapter.



## 7 CPLD

In the simulation and laboratory test phases, there are signal sources in the driver circuits. These should be replaced by a programmable CPLD (Complex Programmable Logic Device), when producing the actual circuit module.

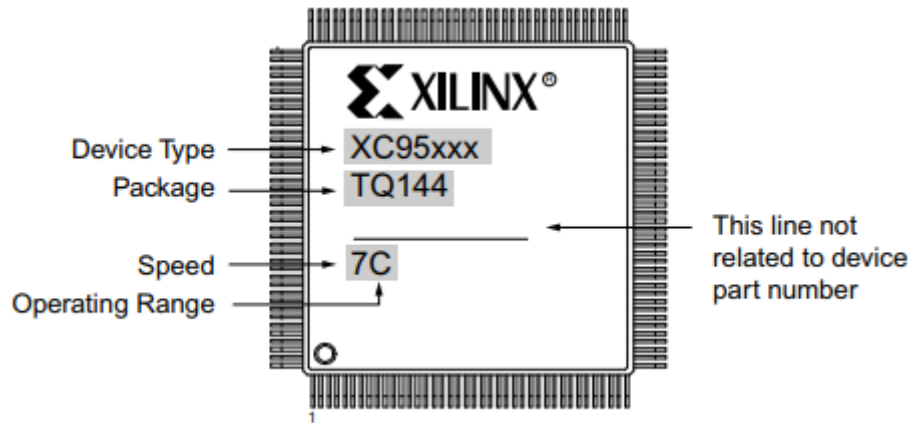


Figure 14 - the XC9572 CPLD, with pins[33].

A CPLD (Complex Programmable Logic Device) is a logic programmable device. Logic functions are controlled through AND/OR arrays, while macrocells is responsible for sequential or combinatorial logic. The CPLD available at school is the XC9572 [33]. A CPLD makes it possible to operate with much higher precision. It is used to create downtime between the SCT3120-transistors in a half-bridge configuration, prohibiting a possible outage of the circuit's voltage source. This device produces very precise signals to the driver circuit and enables the circuits possibility to stop operation if needed.

The CPLD is more accurate than analogue circuits, in control of both dead time and logic protection. The fact that it is programmable, opens the possibility for logic adjustments.

When a CPLD is applied, it will be natural that the dead time and holding circuit of the overcurrent protection are programmed into this.

## 8 Simulation – Single Transistor Driver

The transistor should be tested in a half-bridge circuit.

A simple way of doing this, is by setting up a single transistor driver. It would correspond to a half-bridge configuration, because they have the same set up.

*“The primary function of a drive circuit is to switch a power semiconductor device from the off state to the on state and vice versa.”[26]*

To develop the simulation, simple circuits are constructed, then design improvements are added.

Simulations are performed in OrCAD CAPTURE.

The circuit will be developed based on the following:

1. Ability to change switching speed (For example low current into transistor will cause slow switching speed).
2. As little oscillation as possible (for example regarding the problem of parasitic oscillation).

Ideal values are dependent on the dynamic rise time and dynamic turn on/off delay time given in the transistor datasheet.

The simulation results are saved as a .csv file, which is used in MATLAB to program the projected simulation graphs.

*Note: To avoid misunderstandings, there is no coherence between the colours of the voltage markers and the colours of the graphs.*

# 8.1 Simple Rg driver circuit

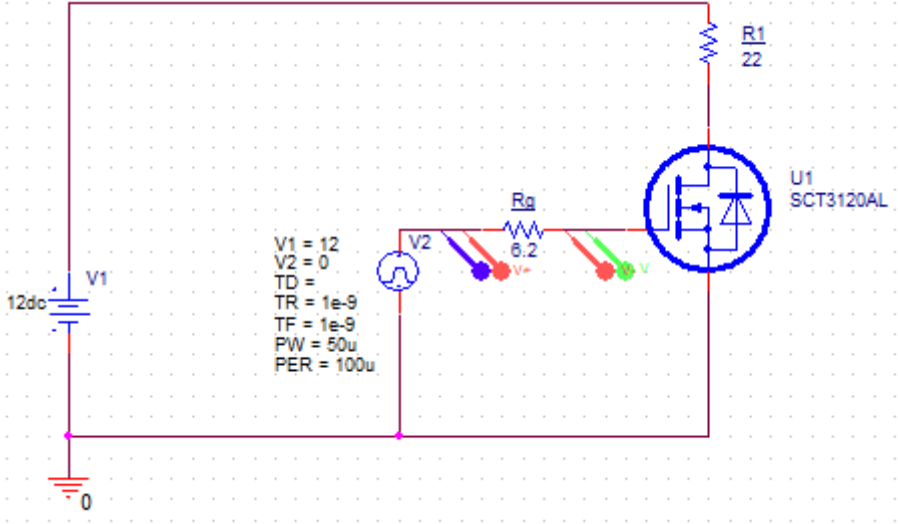


Figure 15 – Simple Rg driver circuit.

Component values were applied to get a valid simulation, so measures were taken to prevent saturation problems. Input sources and components were chosen so that it was possible to use the similar values in the test phase. Thus, comparison would be easier and more viable. The R1 resistor is present to prevent a short-circuit of the source. The circuit has a drive circuit that consist of a simple resistor and source – producing a signal into the base of the transistor.

### Results:

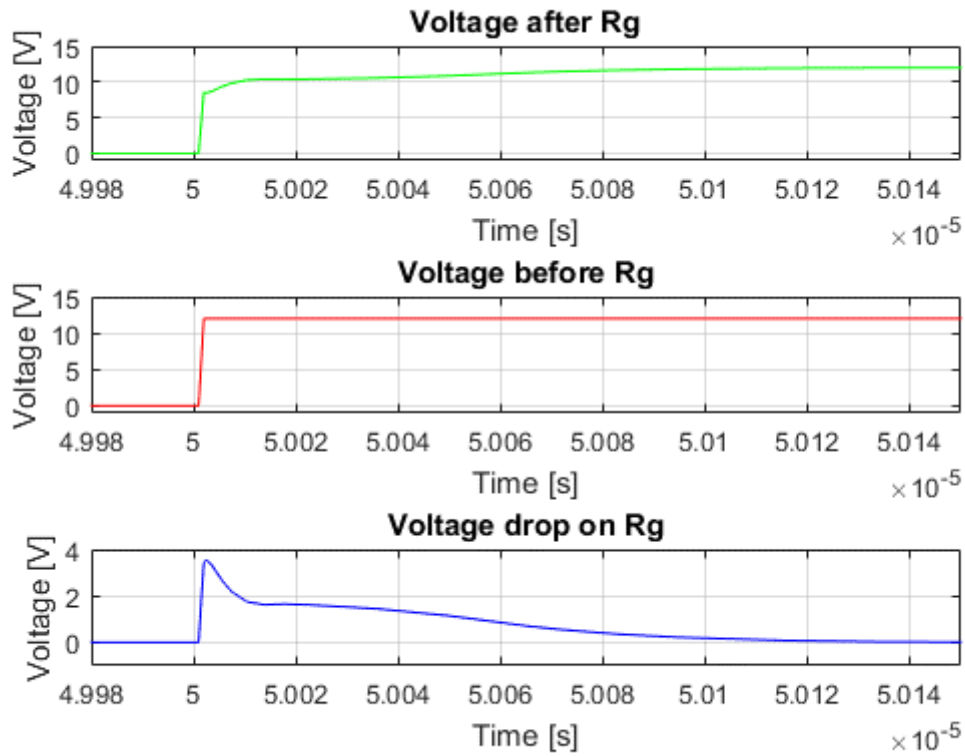


Figure 16 - Single Rg driver circuit simulation results.

Considering the simplicity of the circuit, the switching times are quite good. Though, there is room for improvement on the last part of the rise, on the voltage after Rg. It uses approximately 100 ns to rise fully to 12 V. While the rise to 8 V only takes approximately 1 ns. Notice the lack of voltage oscillation, this is mainly because of the low number of components in the circuit.

**Switching time  $\approx$  100 ns**

## 8.2 Totem pole driver circuit

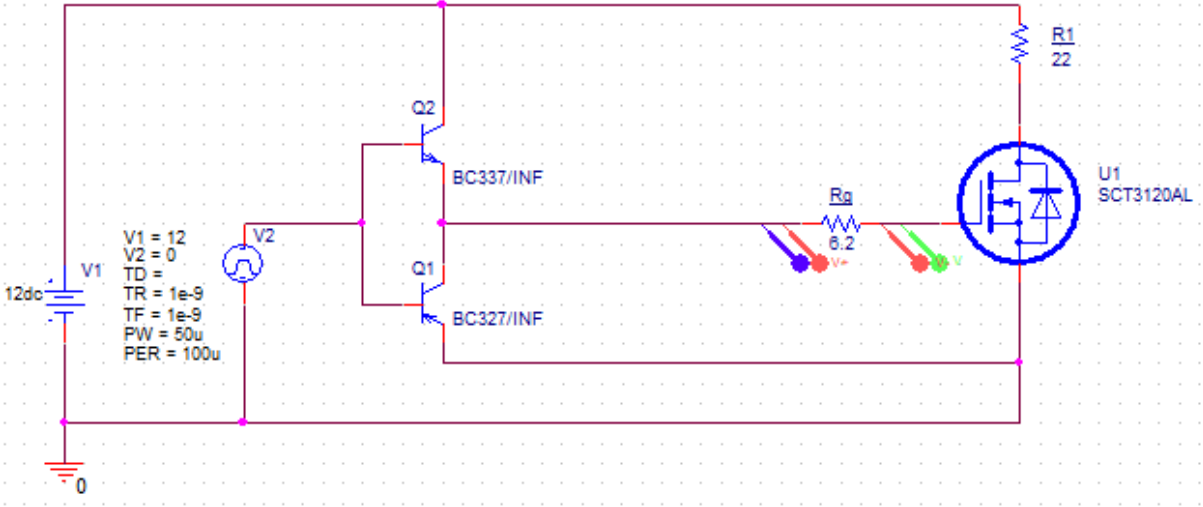


Figure 17 - Totem pole driver circuit.

The main purpose of a totem pole configuration is to enhance the voltage level [26].

In the driver circuit, there are two bipolar transistors connected to the SCT3120AL-transistor gain. One of them are NPN and the other is PNP. Bipolar transistors are used, because a MOSFET transistor must be discharged. This would consequently result in unnecessary delayed switching time.

### Results:

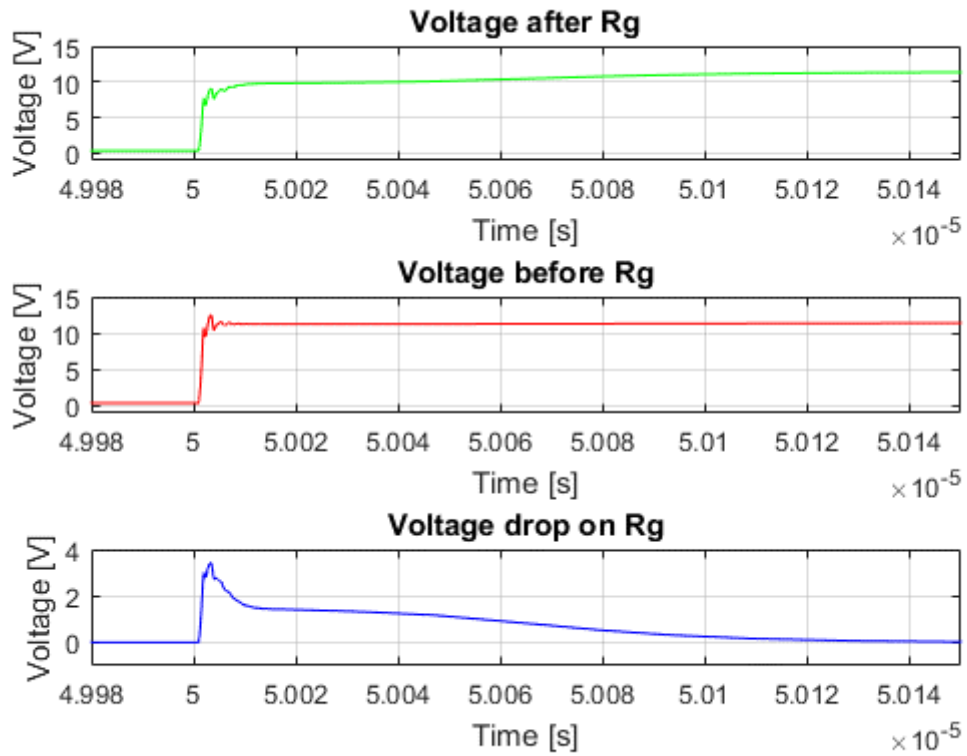


Figure 18 - Totem pole driver circuit simulation results.

The switching time of the totem pole circuit is quite like the Rg circuit. Though, the introduction of the two bipolar transistors in the totem pole configuration has created some oscillations.

**Switching time  $\approx 120$  ns**

### 8.3 Buffer capacitors

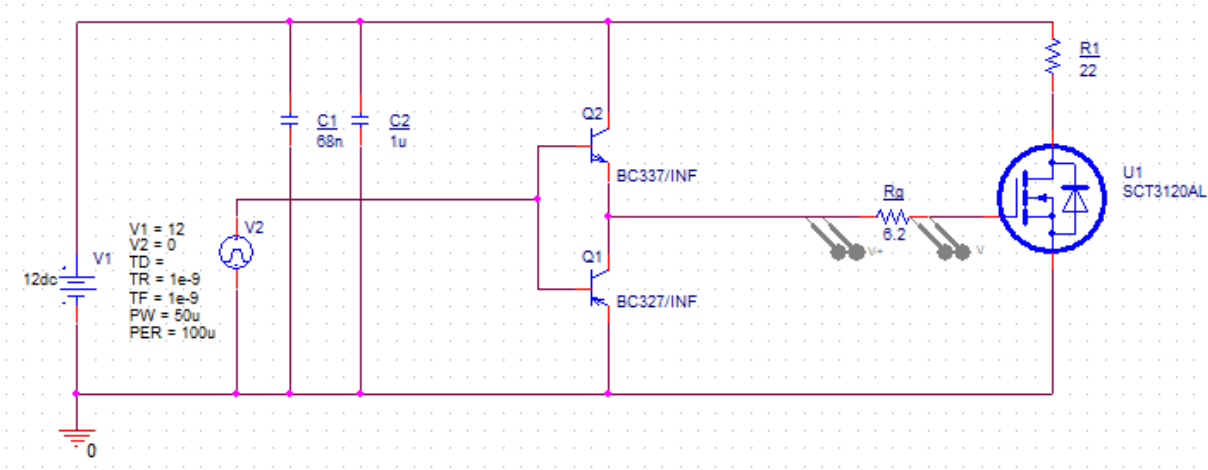


Figure 19 - Buffer capacitors driver circuit.

Buffer capacitors are often applied in such types of situations. One large buffer capacitor to handle the high currents over a longer period. The second buffer capacitor is smaller and used to dampen oscillations of small current peaks, that the large buffer capacitor cannot registrate. A comparison of the oscillations in the totem pole- and buffer capacitor simulations is given in Simulation comparison.

**Results:**

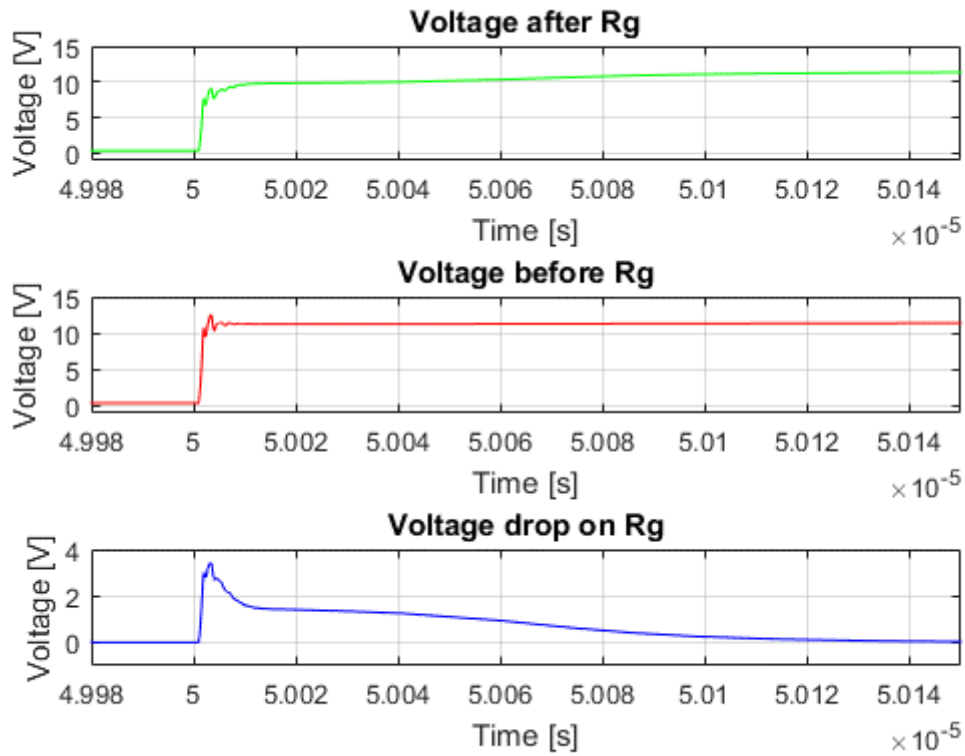


Figure 20 - Buffer capacitors driver circuit simulation results.

**Switching time**  $\approx 125$  ns

It is quite interesting to notice that the buffer capacitors appearance has no significant reaction other than a small increase in switching time. Therefore, a more detailed simulation comparison of the results before and after the buffer capacitors, has been elaborated in Simulation comparison.



## **8.4 Optocoupler**

The absence of pSPICE models for optocouplers has caused the design development in the simulation phase to stop. Several possible optocouplers has been tested, without succeeding. The ideal simulation would be of the HCPL-4200 optocoupler [34], that is used to performed a successful physical test on in Optocoupler. Further design improvements are presented in Experimental results – Single transistor driver.

# 9 Experimental results – Single transistor driver

In this phase, the physical testing of the circuit is presented.

The criterions for the testing phase are the same as for the simulation phase. Meaning results will be judged on switching time and oscillations.

To sustain required gate current on the driver of the wide-bandgap transistor, a separate circuit was created.

The goal of the driver circuit is to provide fast switching speed with as little oscillations as possible, while at the same time keep performances inside the safe operating area of the transistor. Since larger currents is resulting in longer switching times, the goal is to find the exact required current to drive the transistor.

Though the circuits in the simulations and the experimental phase are the same, there are some differences in applying power to the circuit. In this test phase, the switch is connected manually. This can cause delays or unprecise experimental results.

The breadboard was used to couple the circuit, while the power source was feeding it. A signal generated by the oscilloscope was also utilized. Results was observed on the oscilloscope.

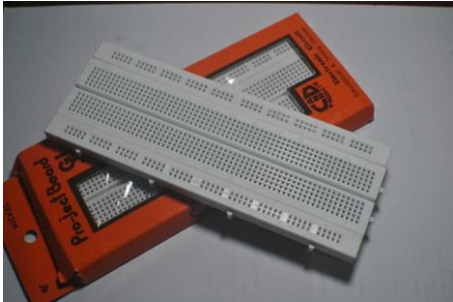


Figure 21 - Breadboard.



Figure 22 – DC power supply.

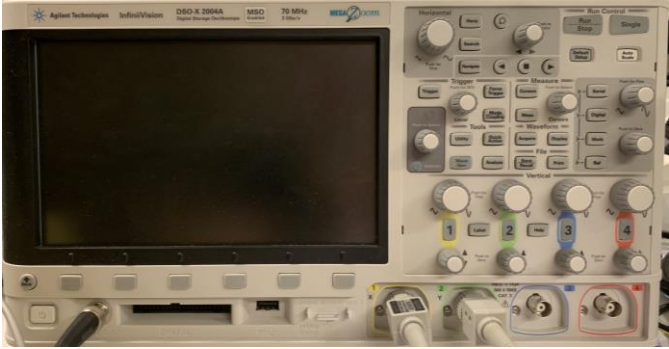


Figure 23 - Oscilloscope.

# 9.1 Simple Rg driver circuit

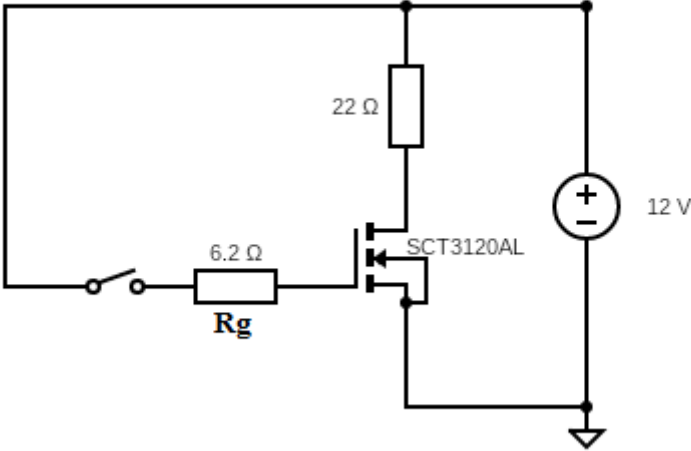


Figure 24 – Simple Rg driver circuit.

In the same way as the simulation, this circuit is constructed to make comparison easy and viable. The 22 Ω resistor is present to prevent a short-circuit form occurring.

### Results:

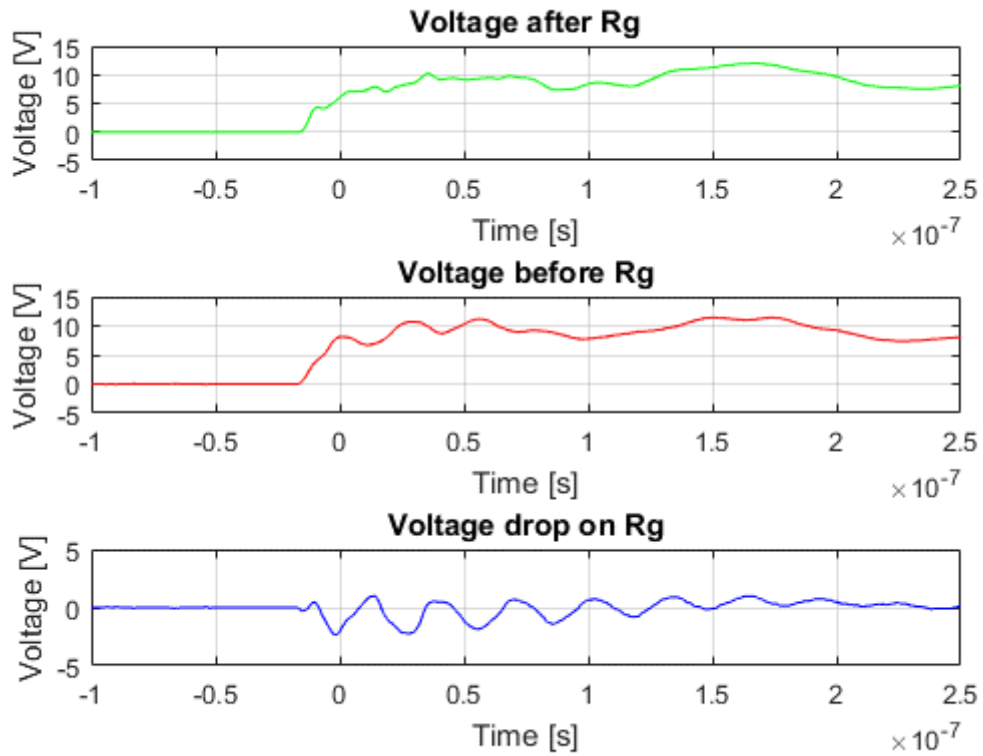


Figure 25 - Single Rg driver circuit test results.

This simple circuit shows fast switching times, mostly because of a small number of components. Though, there are large oscillations present.

## 9.2 Abrade connections

The difference from Simple Rg driver circuit, is solely concerning component connections. The wide-bandgap transistor is abraded so that it fits in the breadboard. Additionally, wires are shortened, and power supply connections are idealized. It is important to minimize stray inductance, to achieve fast switching and avoid switching oscillations.

### Results:

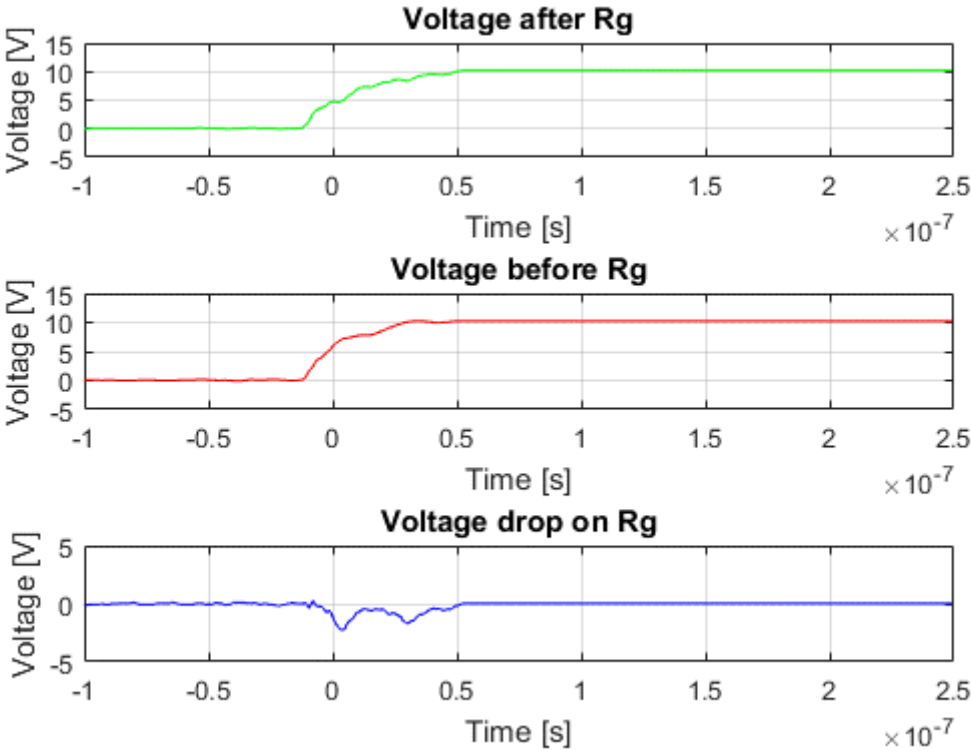


Figure 26 - Simple Rg driver circuit test results with abraded connections.

Because more components will cause more oscillation, future circuit improvements will be a trade of between switching time and switching oscillations.

### 9.3 Totem pole

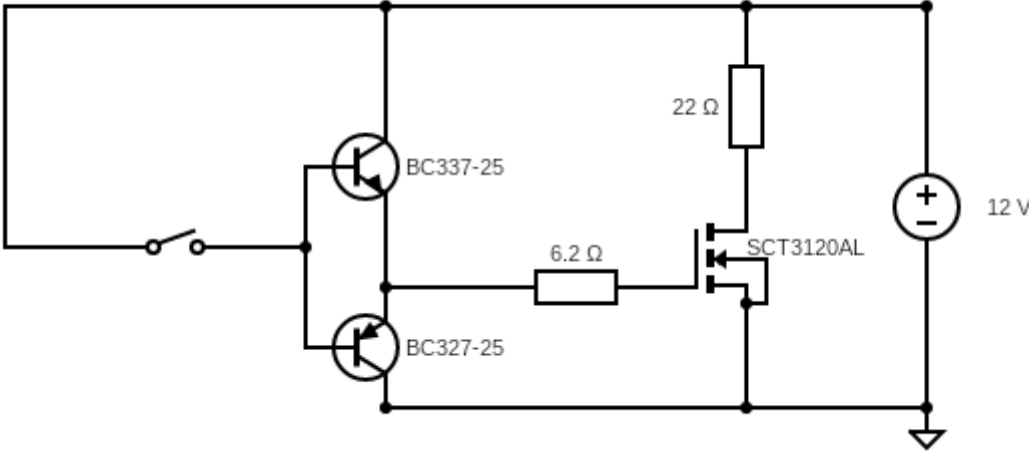


Figure 27 - Totem pole driver circuit.

Bipolar transistors are added to the circuit. This configuration is called a totem pole and works as a way of increasing the power rating. Something interesting to notice is that the switch now does not need to be connected to ground when starting the measuring. This is because the bipolar transistors do not lead current when there is no power supply. During testing, this is observed on the current value of the DC power supply.

**Results:**

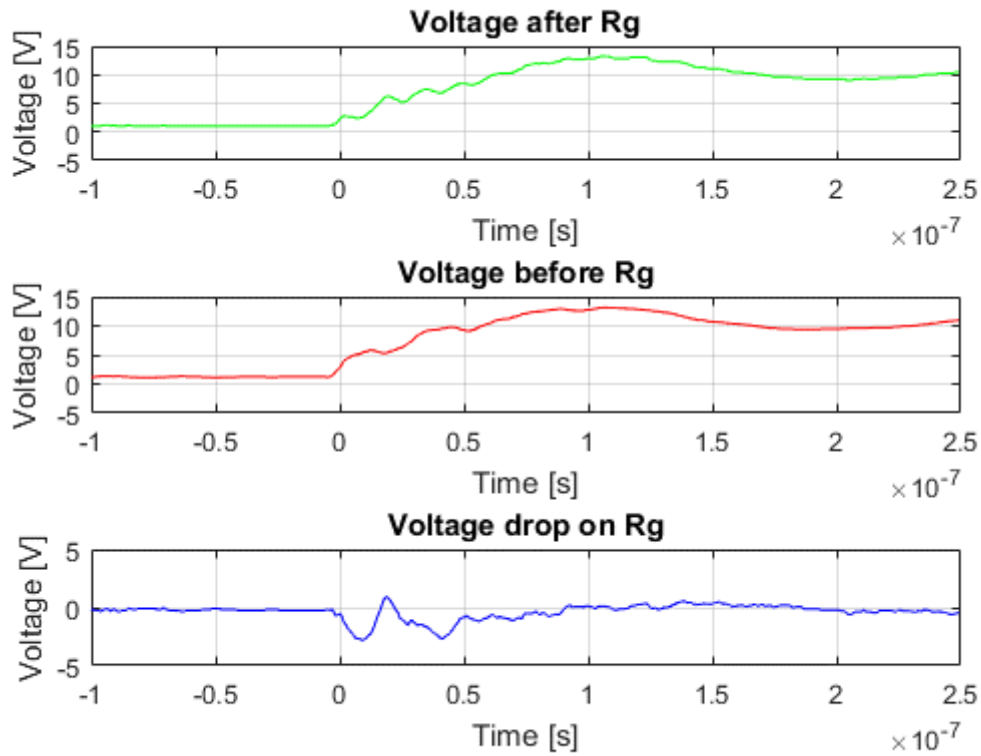


Figure 28 - Totem pole driver circuit test results.

Results proves that that the bipolar transistors 337-25 and 327-25 can handle the current. It is interesting that the switching time has increased while introducing the totem pole configuration. The new total signal delay is equal to the sum of the buffer stage delay and the totem pole switch delay.

### 9.4 Buffer capacitors

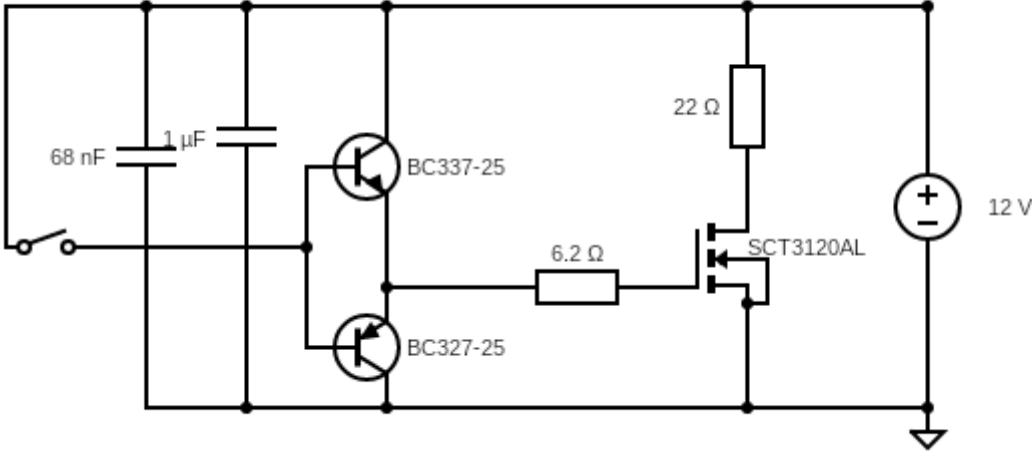


Figure 29 - Buffer capacitors driver circuit.

The collector leg of the NPN bipolar transistor and the emitter leg of the PNP bipolar transistor should be connected to a separate power supply. This figuration should be combined with two buffer capacitors in parallel.

Several buffer capacitors and combinations of them where tested. 56nF, 68nF and 100nF where tested in the circuit as the smaller buffer capacitor. In absence of variations from the testing, the 68nF capacitor was chosen. A 0,68uF and a 1uF electrolyte capacitor was tested in parallel with the 68nF capacitor. Results show a reduction in oscillations and an insignificant performance change in switching time.

**Results:**



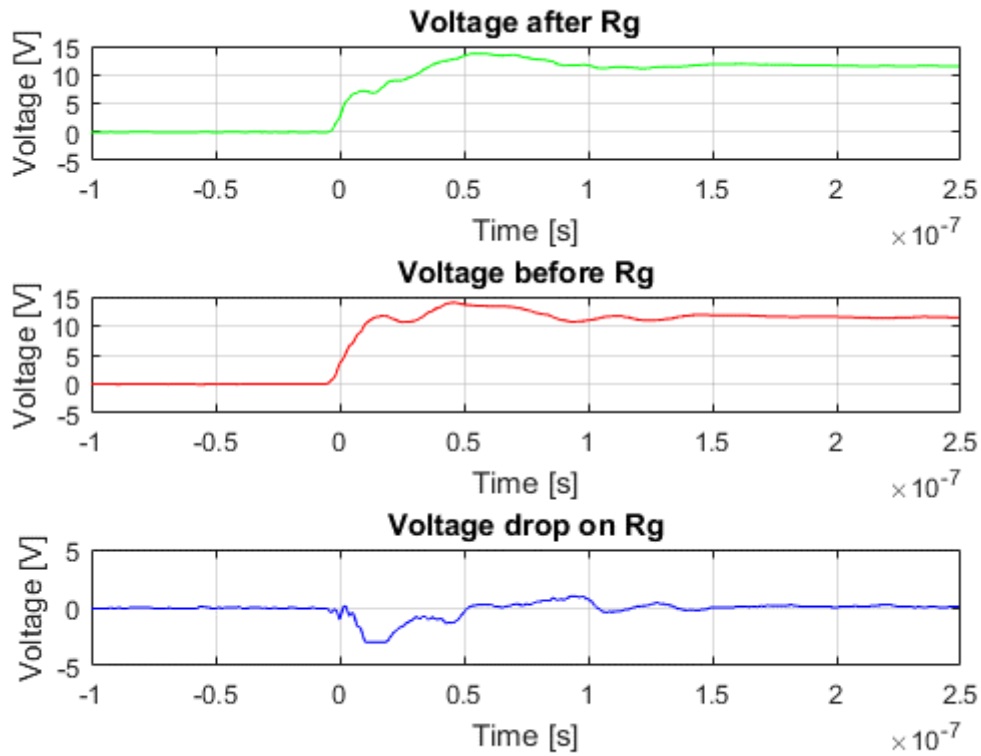


Figure 30 - Buffer capacitors driver circuit test results.

These results imply that the smallest buffer capacitor has removed some of the oscillation. The buffer capacitors were not expected to have this large impact on the switching time, based on results from the simulation. Though, this could be the effect of the manual connection of the switch.

# 9.5 Optocoupler

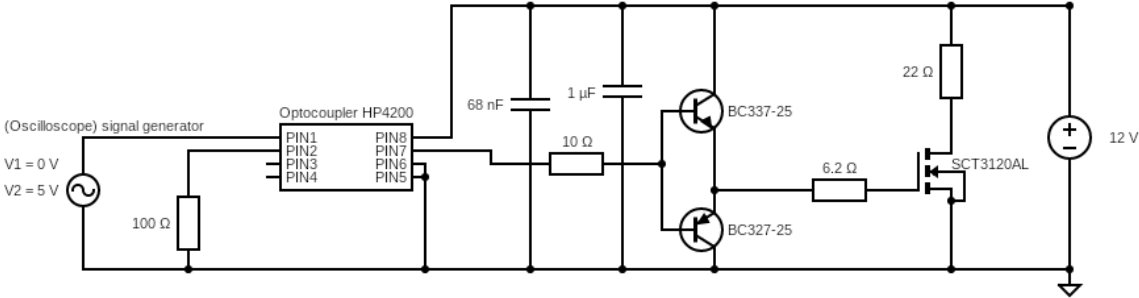


Figure 31 - Optocoupler driver circuit.

A drastic driver circuit improvement is performed by introducing an optocoupler. This device makes it possible to transmit an electrical signal between two isolated circuits, using a LED and a photosensitive device that detects the infrared light from the LED [35].

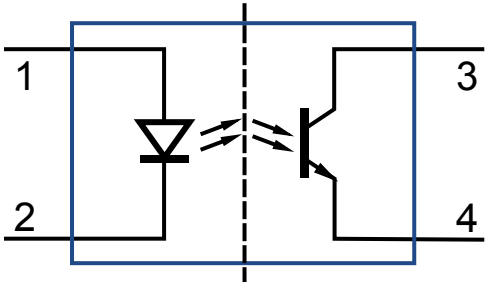


Figure 32 - Optocoupler with LED on the left side, and photosensitive device on the right (without diode, transistor protection and/or amplification) [36].

The purpose of the optocoupler, in this case, is to avoid electrical noise from signals [26]. This is provided by the isolation barrier crossing vertically in the middle of Figure 32 - Optocoupler with LED on the left side, and photosensitive device on the right (without diode, transistor protection and/or amplification) [36]. An optocoupler can secure an external circuit, because hazardous voltages are incapable of penetrating the isolation barrier.

Originally, buffer capacitors were tested in the circuit, to prevent current and voltage spikes. The different values of the buffer capacitors did not show any significant change in results. Therefore, the natural option was to keep the component values from Buffer capacitors.

The absolute maximum ratings in the datasheet stated that the average output current,  $I_o = 25$  mA [34]. This value and the amplification of the bipolar transistors could be used to find maximum gate current.

Using an optocoupler implemented in the driver circuit delays the switching time because of more components. This can be faster with a driver circuit as presented in “A New High Efficiency Current Source Driver With Bipolar Gate Voltage”[37]. This method can turn off the MOSFET much faster with a high effective gate current.

Development in the circuit configuration is causing the switching time to be much higher. The main reason for this is the propagation delay given in the switching specifications in the optocoupler datasheet [34]. Preferably a rise time of approximately 400 – 500 ns would be ideal.

**Results:**

*(Notice the change in results graph parameters)*

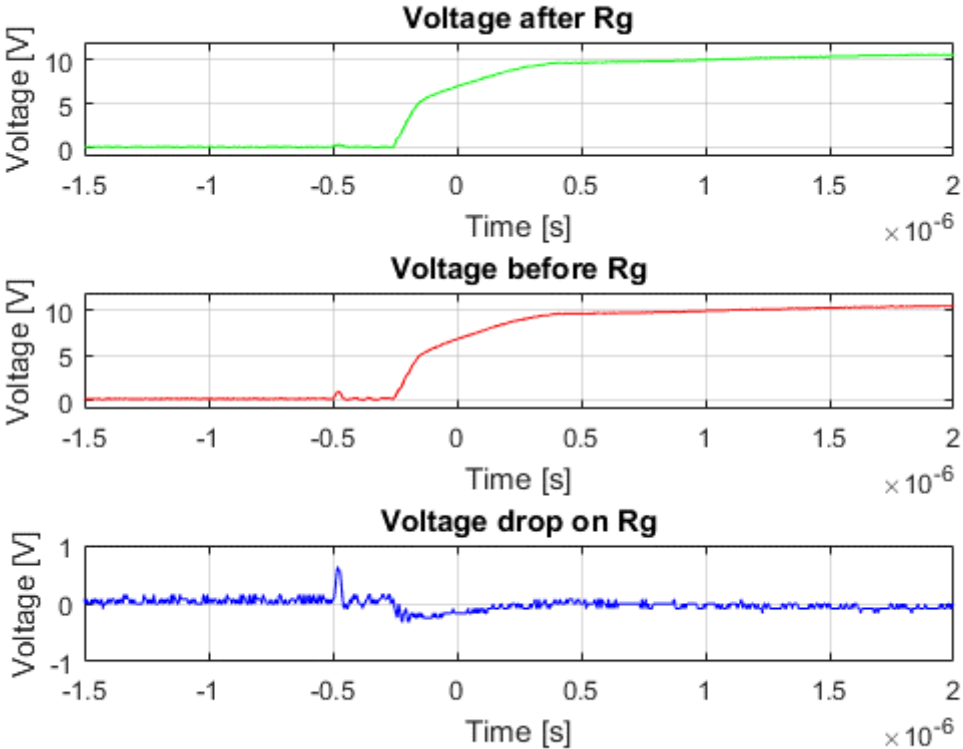


Figure 33 - Optocoupler driver circuit test results.

It is observed that the totem pole optocoupler configuration starts the voltage drop before the other tests. Though, there is still expected time delay before voltage capability is reached. Notice the voltage top that reaches maximum 10-11 V. This is because of the characteristics of the optocoupler[34].

As we can observe from the test, the rise time is approximately 1700 – 1900 ns. One can argue that this delay is affected by the connection between components and current supply. But there is also room for improvement in circuit composition.

### 9.6 1 $\mu\text{F}$ capacitor

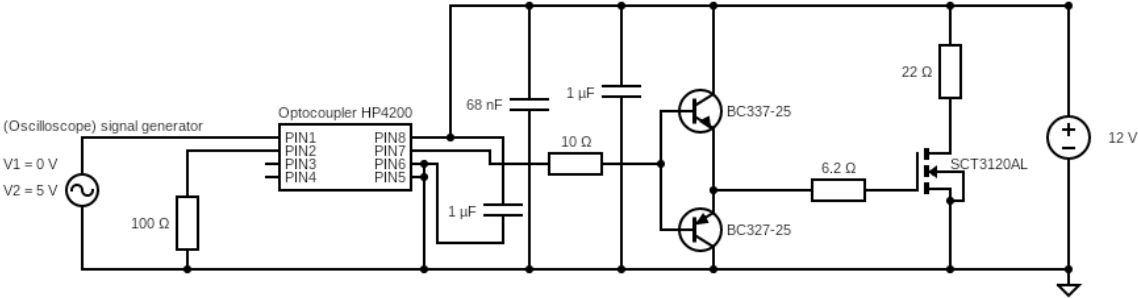


Figure 34 - 1  $\mu\text{F}$  capacitor driver circuit.

Based on the similarities in circuitry from the HCPL-2200[38], and ACPL-343 datasheet [29], a 1  $\mu\text{F}$  bypass capacitor was added between the eight and the sixth leg of the optocoupler. A bypass capacitor removes AC signals that are present on a DC signal by connecting them to ground.

**Results:**

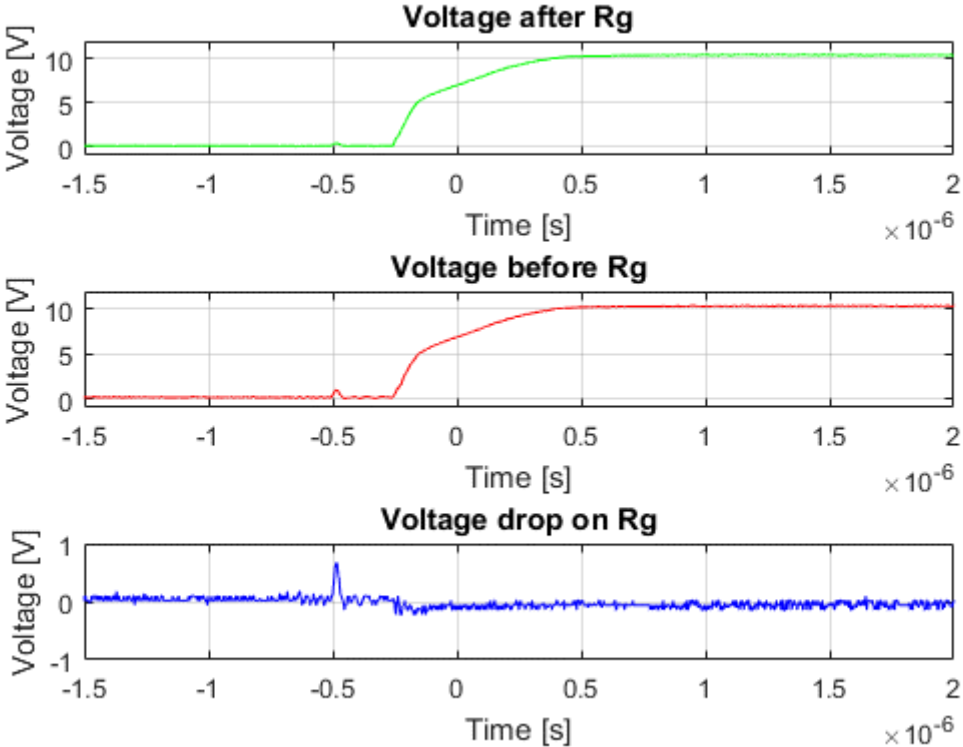


Figure 35 - 1  $\mu\text{F}$  driver circuit test results.

As results show, the switching reaches the penultimate voltage levels much faster with than without the capacitor. It is reduced to approximately 1000 ns. Oscillations are now almost non-existing on the rise.

## 9.7 Rg update

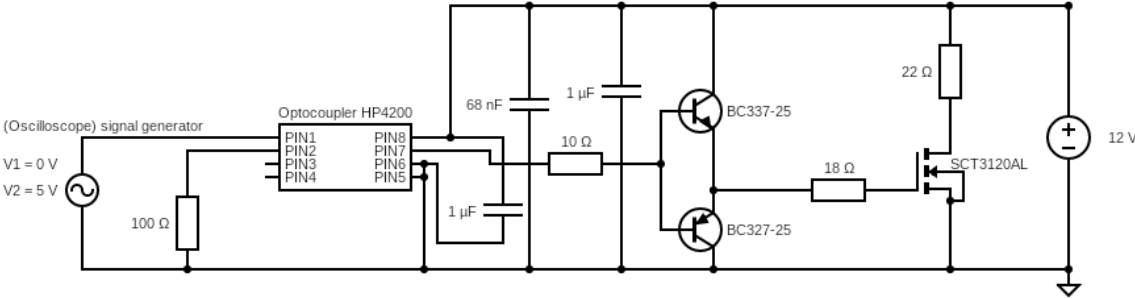


Figure 36 - Rg update driver circuit.

This step is a simple exchange of Rg resistor, that has had the value of 6,2Ω. Based on the information from the SCT3120AL datasheet [21] this resistors value should be 18Ω.

**Results:**

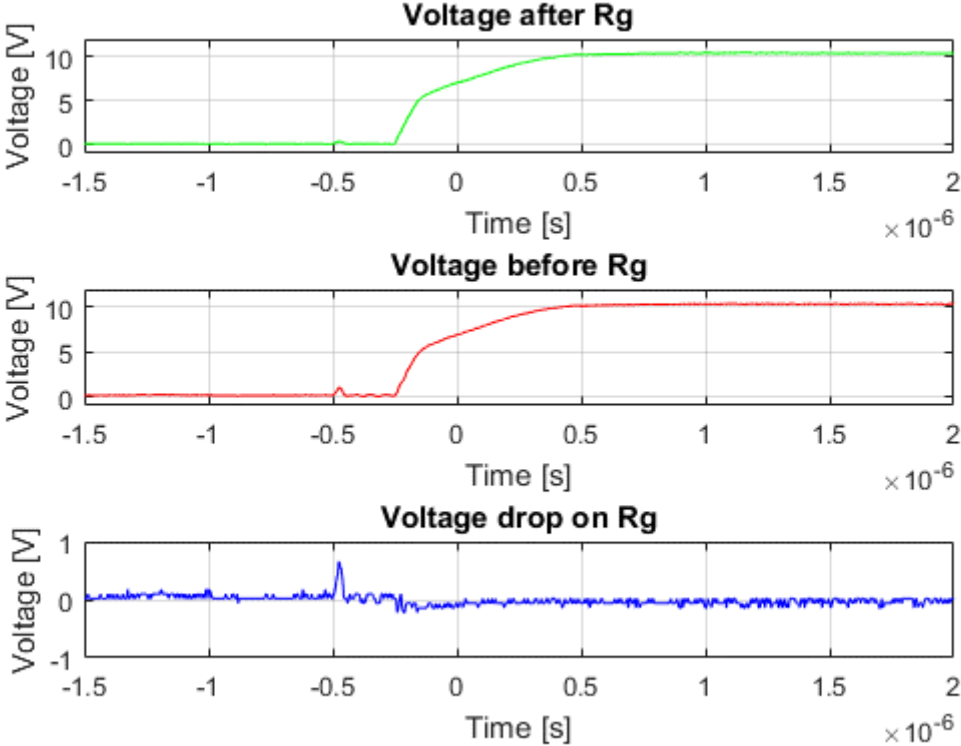


Figure 37 - Rg update driver circuit test results.

As measurements show, the resistor change does not affect the simulations very much. Switching time  $\approx$  1000 ns.

## 10 Further improvements

### 10.1 Snubber circuit

A snubber circuit should be introduced. The reason why this is done, is because it absorbs energy from the circuit's inductance, when the switch is opened. In other words, the voltage- and current spikes on the simulation/experimental phase would be decreased when switching. The snubber circuit is connected between the drain- and source leg of the WBG transistor. It must be located physically as close as possible to the device to minimize stray inductance effects.

When the transistors works as a switch, it can be affected by rapid rise of voltage across the device at turn-off, and possible rapid rise of current at turn-on. These rapid changes can be reduced by the snubber circuit presented in Figure 38 - Snubber circuit in bridge configuration [26].

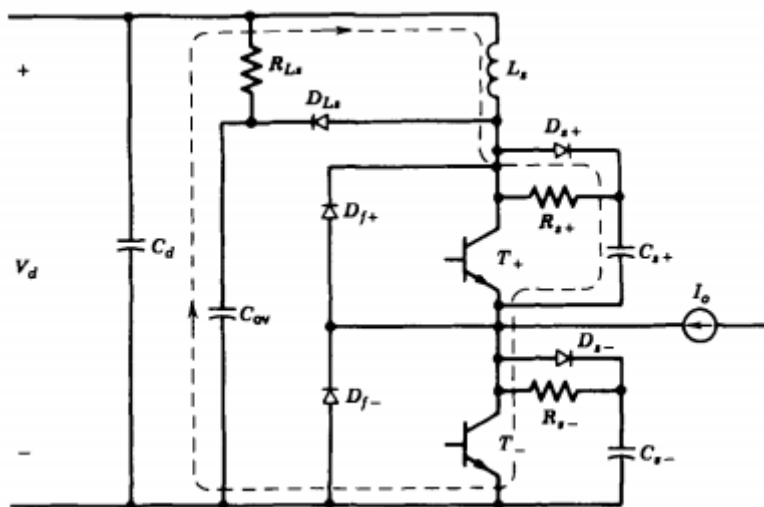


Figure 38 - Snubber circuit in bridge configuration [26].

It is normal with a diode in the snubber circuit, so that it would not be any power loss when the transistor is open. The use of snubber networks is many, because they are used for circuit protection, sharpening voltage- and current waveforms and for making transient overshoots less severe [6].



## 10.2 Dead time implementation method (RCD)

RCD delay circuit could be tested as a separate circuit, by comparing voltages in and out from the circuit. This type of circuit could be coupled directly between gate and source or integrated in the driver circuit.

### Test:

The dead time circuit is independent from other circuitry and is set up as shown in Figure 39 - RCD dead time test implementation circuit. Several components (R1 and C1) should be tested to secure the most ideal dead time.

The optocoupler is the same as in the single transistor driver circuit. While a valid comparator could be the LM339N [39], that already is available from UiT Narvik.

The dead time should be longer than the time it takes for the transistor to turn off. The voltage on the plus terminal of the comparator should be simulated or calculated. Analyses should be done on the rising characteristics of the transistor, then choose the voltage that is cohering to its turn-off time. This is the value that should be given to the variable source.

The switch is implemented as an option, if dead time should not be necessary.

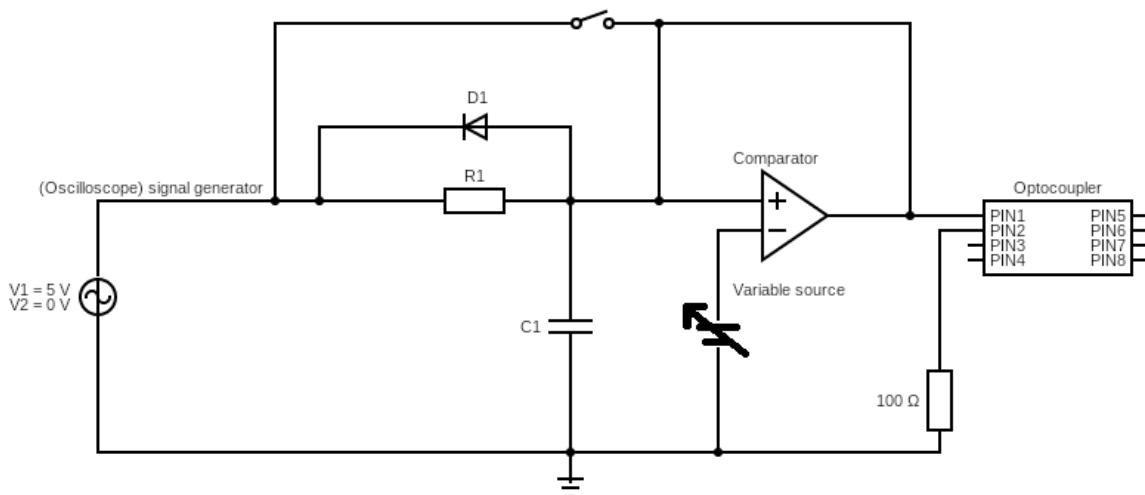


Figure 39 - RCD dead time test implementation circuit.

*Note: test has not been performed on this circuit, as there was no available time to do this before the thesis deadline.*

### 10.3 Over current protection – Second order RC-circuit

To implement over current protection, an opportunity is to do like it has been done in “Comparison of two gate drivers for SiC MOSFETs on switching performance and over current protection” [40]. Here, a second order R-C circuit is developed to detect over current.

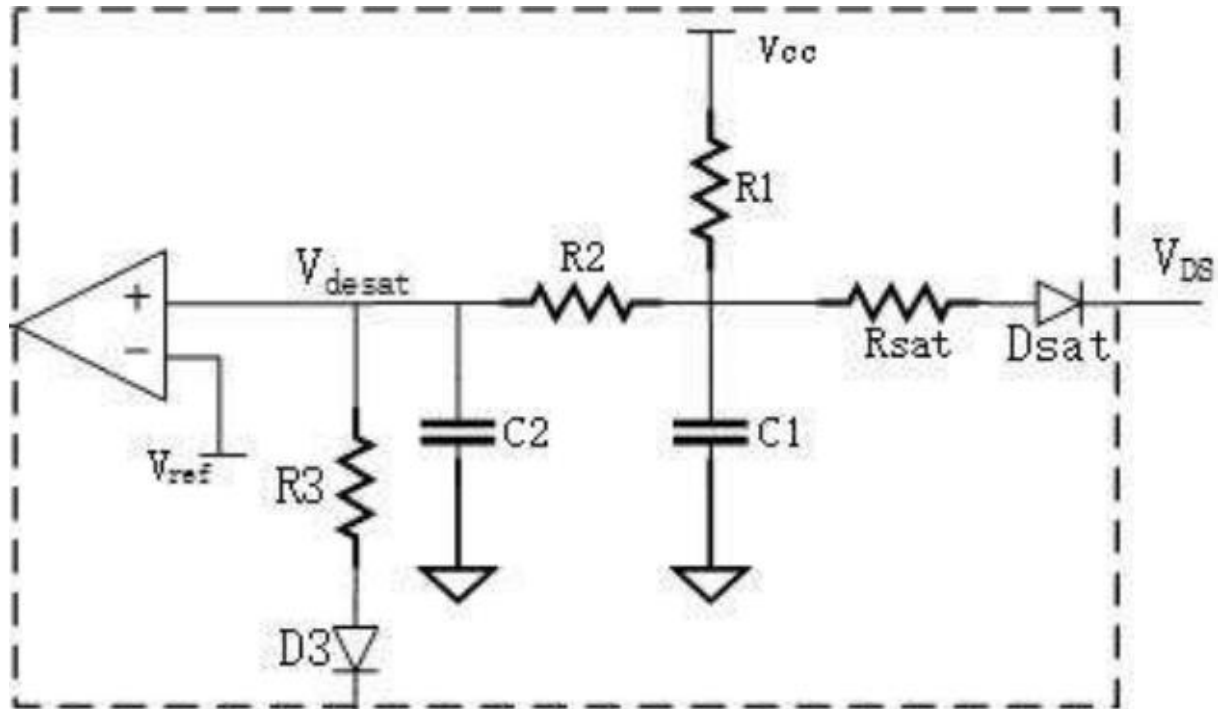


Figure 40 - R-C over current detection.

The D3 diode is connected directly to the gate. The triangular component in Figure 40 - R-C over current detection, is a comparator. It uses an operation amplifier to compare the voltage magnitude on the two inputs. Then it determines which of the two is the largest one. In other words, a fault will be present at the output of the comparator, when  $V_{desat}$  is larger than  $V_{ref}$ .

A holding circuit is required to avoid that the protection automatically resets when the current drops below the threshold. Possible faults should be cleared, and the circuit should be reset. If the circuit restarts and experience the same fault repeatedly, it would eventually be damaged or in worst case be destroyed.

A holding circuit uses so called SR-latch (see Figure 41 - SR-latch [41]). Its output signal is inverted, meaning that an AND gate could be used with input signals from comparator output and signal generator.

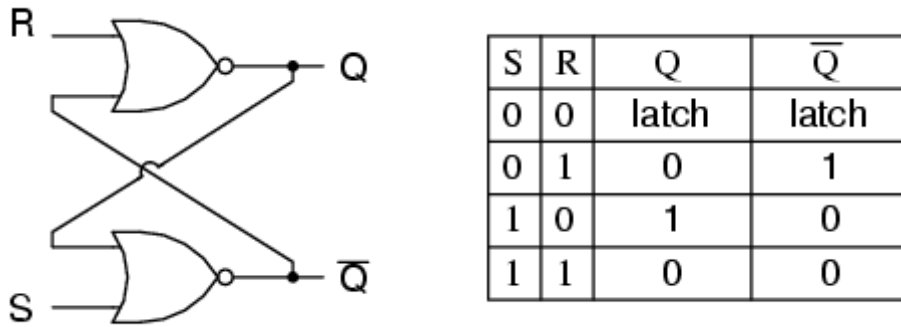


Figure 41 - SR-latch [41].

### 10.3.1 What happens when fault occurs

In the overcurrent protection circuit,  $V_{desat}$  is suddenly higher than  $V_{ref}$ .  $V_{desat}$  is chosen as output by the comparator, indicating fault. As a result, the SR-switch is enabled in the holding circuit, inverting the high signal to a low signal. This forces the output of the AND gate to go low (see Figure 42 - AND gate).

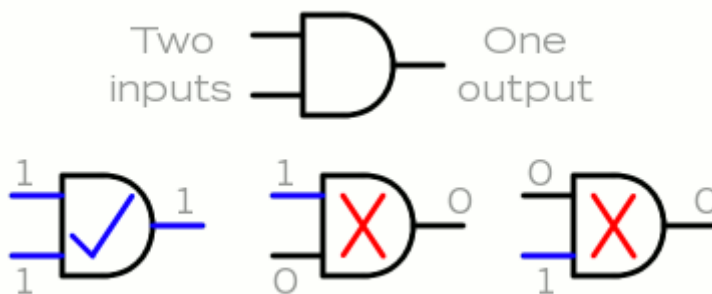


Figure 42 - AND gate [42].

## 10.4 Final half-bridge module

After developing and verifying the single transistor driver circuit, over current protection, snubber circuit and dead time, it would be natural to construct a half-bridge module. In the project assignment, the following is stated:

*“In this project a half-bridge should be designed as a building block for power converters based on wide-bandgap transistors in converter applications.”*

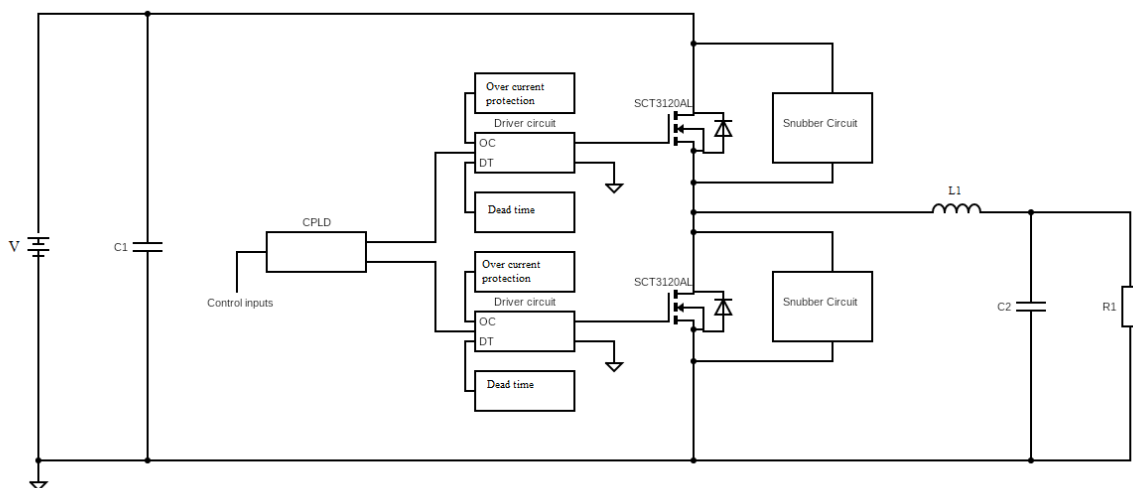


Figure 43 - Final half-bridge module.

The above circuitry is a half-bridge buck configuration.

An alternative circuit configuration during testing could be to apply two voltage sources to activate the usage of the second WBG-transistor. This means that the C2 capacitor would not be necessary, therefore it could have been removed. Normally a diode would be utilized in a boost circuit, but this can also be removed when two voltage sources is applied. The R1 resistor should be coupled directly between the two voltage sources. The inductor should also be moved in case of a boost converter.

Note that when the CPLD eventually will be a part of the circuit, dead time and the holding circuit of the over current protection is implemented in it. These parts are separate in Figure 43 - Final half-bridge module., because it is not a part of the thesis to programme the CPLD.

# 11 Discussion

This chapter consist of comparisons of the simulation and the experimental phase, both internally and between each other. Some similarities are observed, which again undergird the demand for abraded connections between components. This is incredibly important in a system that serves with optimal efficiency.

Looking back, calculations should have been performed, to find the most suitable optocoupler for the single transistor driver circuit. This would have idealized the efficiency of the circuitry. The absence of pSPICE simulation file for the HCLP-4200 optocoupler is unfortunate. Though, the optocoupler experimental phase confirms that the HCPL-4200 is a natural circuit development to implement. The lack of oscillation is very promising, though there is still room for improvement concerning switching time. This is somewhat improved by the capacitor added in 1  $\mu$ F capacitor.

## 11.1 Simple Rg

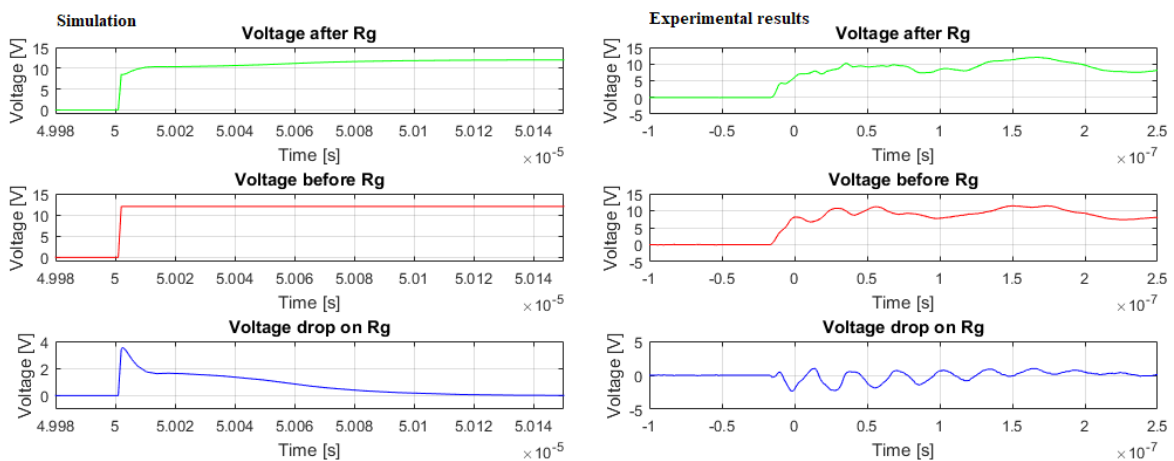


Figure 44 - Simple Rg driver circuit – simulation and experimental results compared.

Large oscillations during voltage rise is observed in the experimental results. Also notice the dip in voltage level after reaching 12 V. The abraded connections and a very precise test are performed in Abrade connections - where the similarities to the simulation is astonishing.

Significant differences in voltage drops is observed, due to an imperfect control signal (before Rg).

# 11.2 Totem pole

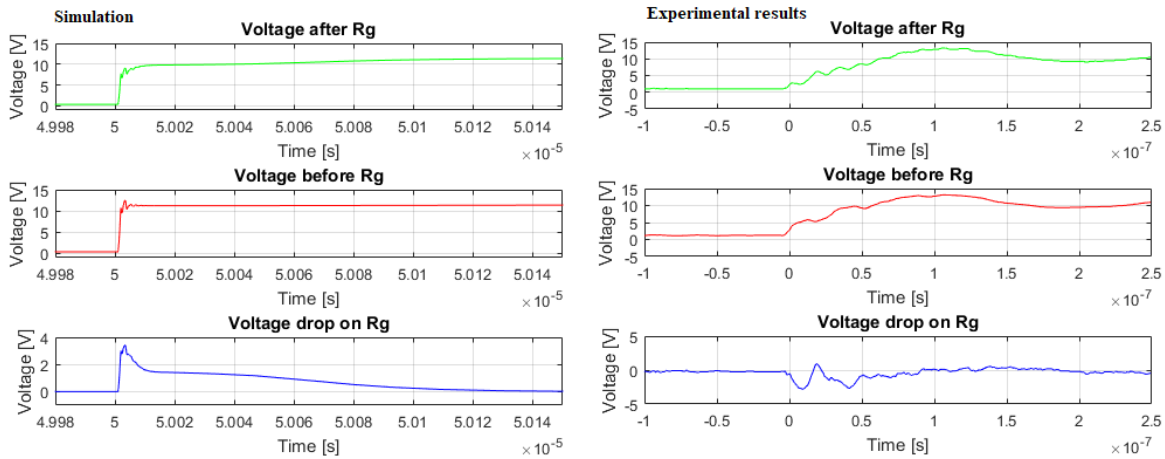


Figure 45 - Totem pole driver circuit – simulation and experimental results compared.

The simulation has a switching time of around 120 ns, while the experimental results show a switching time of around 100 ns, to reach the full voltage level. Though, approximately 80% of the rise in the simulation happens in 3-5 ns, which is very rapid. Other remarks are the slight dip in the experimental results. This could be caused by inaccurate testing conditions, or it is an indicator that circuit improvements are needed.

### 11.3 Buffer capacitors

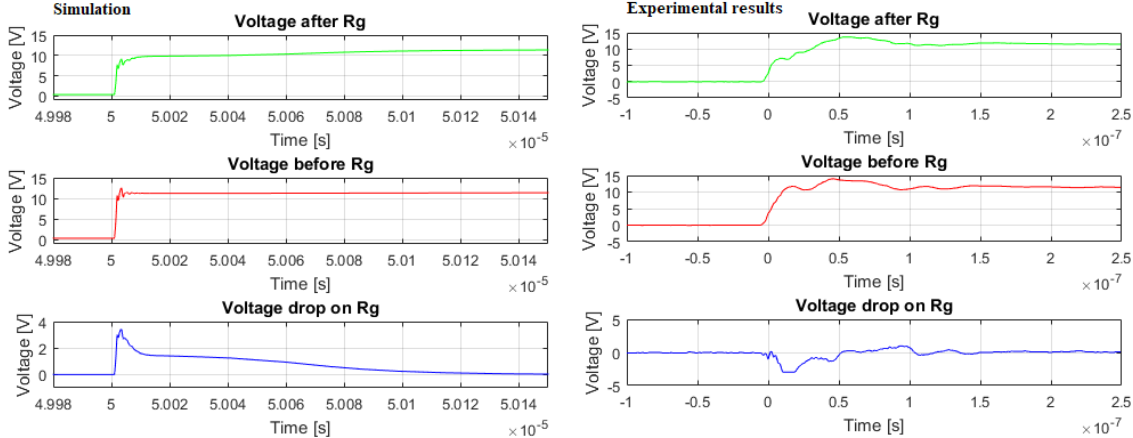


Figure 46 - Buffer capacitor driver circuit – simulation and experimental results compared.

The introduction of the buffer capacitors has had no significant impact on the simulation. Whilst in the experimental results, the dip described in Simple Rg and

Totem pole is almost non-existing.

### 11.3.1 Simulation comparison

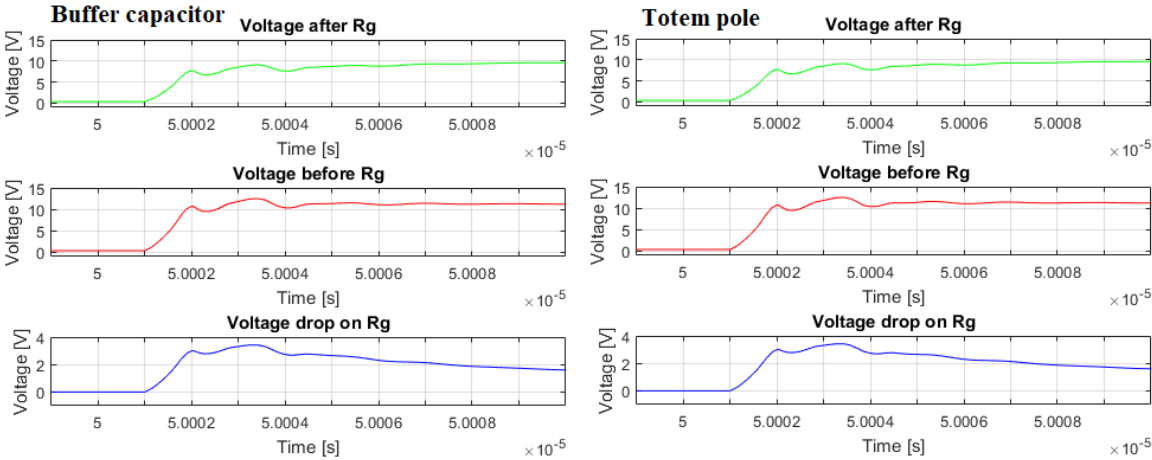


Figure 47 – Comparing oscillations in totem pole- and buffer capacitor simulations.

These simulations needed a closer look. Though, the simulation say that the buffer capacitors still should not provide any difference in oscillation. This is quite interesting, because we can see a clear difference from the experimental phase, Buffer capacitors.

### 11.3.2 Simulated Vds

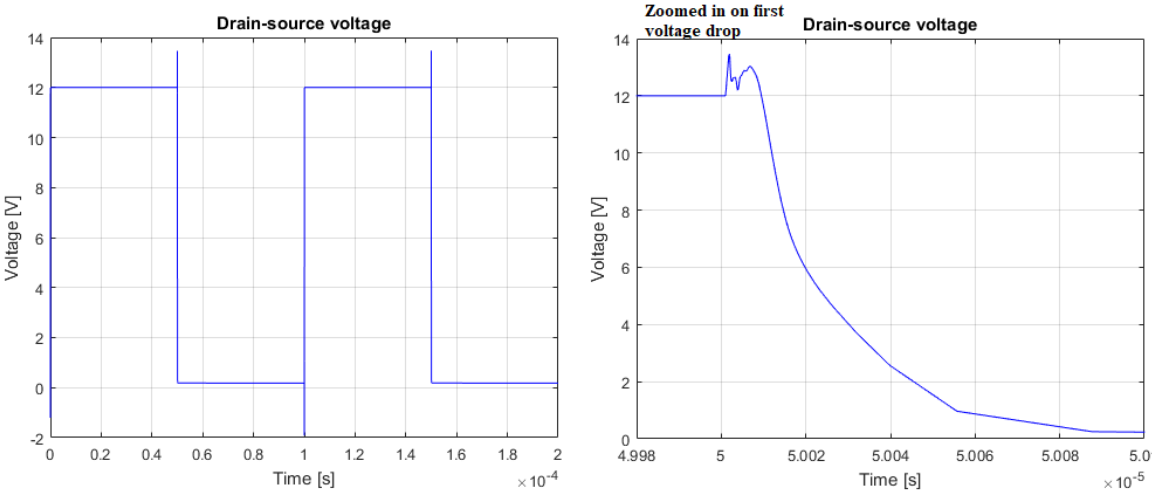


Figure 48 - Buffer capacitor simulating results of Vds.

The drain-source voltage is presented to verify the simulation. Vds is checked after design improvement, and the results are the same as in Figure 48 - Buffer capacitor simulating results of Vds. , for each step. This means that the design upgrades of totem pole- and buffer capacitor configuration, has not reduced the transistors performance.



## **12 Conclusion**

The possibilities of WBG devices in modern technology are fundamental and diverse. Due to faster switching, reduced losses, increased power density and higher operating temperatures, WBG devices can fulfil increased energy needs by reducing energy use and system cost.

This thesis shows that it is possible to design a half-bridge building block for power converters using WBG transistors. However, there are challenges in finding ideal circuit solutions. Small design changes can cause vast differences in resulting characteristics.

Simulations and experimental results show that switching time and oscillations can be minimized by implementing the driver correctly.

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