

A Novel Technique to Mitigate the Overlap-Time Effect in Current Source Inverters

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Abstract— Generally, the current source inverter is considered more reliable than the voltage source inverter due to the presence of inductor as an energy storage element on the DC link, but a disruption in the inductor current could significantly risk its reliability. To guarantee the reliable operation of current source inverter, an overlap time must be added to the gate signals of its switches. This ensures the safe operation of current source inverter but results in increased total harmonic distortion and reduction of DC current utilization ratio. This paper proposes a new technique for reducing the effect of overlap time and improving the performance of pulse width modulated current source inverter. The proposed technique modifies the level-shifted sinusoidal pulse width modulation to mitigate the effect of overlap time. In this paper, the working principle of the proposed technique is presented in detail, and a mathematical relation between the level shifting and overlap time is established. Moreover, a function for the approximation of output AC current is also presented. Finally, results from computer simulations and experiments are presented which validate the effectiveness of the proposed technique.

Keywords— Current source inverter, pulse width modulation, overlap time, harmonics, DC link current utilization.

I. INTRODUCTION

In the past few decades, the voltage source inverter (VSI) has gained a lot of attention from researchers and industry due to the vast availability of voltage sources and suitable switches and its better efficiency. On the other hand, the current source inverter (CSI) could not catch much attention due to the unavailability of switches with reverse voltage blocking (RVB) capability and a bulky energy storage device, i.e., DC link inductor. However, CSI has some unique features that VSI lacks, including inherent boost capability, short-circuit protection, and near-sinusoidal output voltage.

Several solutions have been proposed to mitigate the above-mentioned issues of CSI. To enhance the RVB capability of semiconductor switches like metal oxide semiconductor field effect transistor (MOSFET) and insulated gate bipolar transistor (IGBT), a series connected diode is considered a conventional solution. The series connection of diodes increases the component count, cost, and losses, and it degrades the performance of CSI. A reverse blocking (RB) IGBT was also developed, which reduced the conduction losses, but it could not gain much attraction due to the poor switching behavior of its intrinsic diode [1]. A few bidirectional (BD) switches have also been developed, in which series diode is replaced with another anti-series connected active switch. These kinds of BD switches have RVB capability equal to the forward voltage blocking capability of the active switch, improved dynamic performance, and reduced conduction losses [2]. Two discrete

switches (Si/SiC MOSFETs or GaN high electron mobility transistors (HEMTs)) could be connected in two different configurations, i.e. common source configuration and common drain configuration to develop a BD switch. A few monolithic BD switches have also been developed [3], [4], but they are not commercially available.

As mentioned earlier, the DC link inductor has been a major contributor to the size, weight, and efficiency of CSI, which has limited its wide adoption. Despite its effect on the size and weight of CSI, the DC link inductor of CSI is considered a more reliable energy storage device than the DC link capacitor of VSI, especially in high temperature applications. Moreover, wide bandgap (WBG) switches also have high temperature tolerances, lower conduction losses, and the ability to operate at high switching frequencies. The use of WBG switches, especially BD WBG switches, could significantly improve the performance of CSI and reduce the size and weight of its DC link inductor. Adoption of WBG switches makes the CSI capable of surpassing VSI in reliability, efficiency, and power density [5].

Unlike the CSI, the DC link capacitor is used in the VSI as an energy storage device, so a short-circuit could damage its switches due to the high current. To avoid short-circuit conditions, dead time or blanking time is added to the switching patterns of its switches. CSI has an inductor as an energy storage device, so in case of short-circuit, the inductor limits the current, but for the reliable operation of CSI, open-circuit conditions must be avoided. If the inductor current is disrupted, the inductor will induce a high voltage, which could destroy the switches. For this reason, an overlapping time or anti-dead time must be added to the gate signals of its switches, which will ensure that the open circuit condition is avoided. Insertion of overlapping time guarantees the reliable operation of CSI, but it has adverse effects on the output current, i.e., it increases the total harmonic distortion (THD) and reduces the magnitude of AC current.

There are different modulation techniques that generate the switching patterns for the switches of CSI, like space vector modulation (SVM), selective harmonic elimination (SHE), carrier-based sinusoidal pulse width modulation (SPWM), etc. Due to the need for overlapping time, most of the carrier-based modulation techniques suffer from complexity as they require logic mapping to make the pulse width modulation (PWM) techniques of VSI usable for CSI [6–8]. Several articles discuss the effect of dead time on the performance of VSI and techniques to mitigate it [9–12]. There are a few articles that focus on the effect of overlapping time and its mitigation, but these techniques require AC voltage measurement [13–14]. Suroso et al. [15] propose an overlapping time compensation technique that does not require any measurements of AC voltage. This technique

reduces the THD by using four carrier signals; two of these carrier signals need shifting and scaling, which complicates the implementation. Moreover, in [15], the relation between overlap time and percentage of compensation or intersection is not presented, but results show that percentage of compensation and overlap time have a nonlinear relationship, so controlling overlap time becomes challenging. Additionally, the DC current utilization ratio (DCUR) of the proposed technique is not discussed in [15].

In this paper, a novel technique is proposed to mitigate the overlap time effect for PWM CSI. This technique equips the level shifted SPWM with a new and effective method of overlap time effect suppression without using any information of AC voltage. In the proposed technique, all the carrier signals have the same amplitude, which makes the establishment of the relation between level shifting and overlap time simple. The proposed overlap time suppression technique guarantees the reliable operation of CSI and keeps the THD low. The proposed technique fully retrieves the lost current pulses, thus improving the DCUR and decoupling the control of current from the overlap time. To validate the performance of the proposed overlap time effect suppression technique, it is simulated using MATLAB-Simulink, and results are compared with the conventional technique. The results show that the proposed technique reduces the THD from 12.08% to 2.06% at unity modulation index and at lower values of modulation index i.e. at 0.7 and 0.4, it reduces the THD (%) by 7.26 and 10.62 times, respectively. Moreover, experimental results are also presented that are in conformance with the simulation results, but due to the limited current rating of the DC link inductor, the experimental setup is tested with low current.

II. OVERLAP TECHNIQUES

To analyze the performance of conventional and proposed overlap techniques, a single-phase H-bridge CSI is used. The circuit configuration of the single-phase H-bridge CSI is depicted in Fig. 1, where a DC voltage source (V_{in}) and a DC link inductor (L_{dc}) are connected in series to create a DC current source. To enhance the RVB capability of MOSFETs (S_1, S_2, S_3, S_4) of CSI, a diode is connected in series with each MOSFET. CSI converts the DC current into PWM current, and the output capacitor (C_f) acts as a filter and provides smooth voltage and current to the load. For the safe and reliable operation of this CSI, the DC link current (I_{dc}) must be continuous. To keep the I_{dc} continuous, an overlapping time (T_{ov}) must be added to the gate signals of switches of CSI. This enhances the reliability of CSI.

For demonstration purposes and to evaluate the performance of conventional and proposed overlapping techniques with controlled I_{dc} , controlled current source is used in simulations. However, in the experiments, the circuit shown in Fig. 1 is used.

A. Conventional Overlapping technique

The conventional method to generate the overlap time is based on the insertion of an off delay into the gating signals of the switches of CSI, which was proposed in [16]. This section analyzes the behavior of CSI with conventional overlapping technique. For simplicity, the switches S_2 and S_4 are supplied with PWM signals, while switches S_1 and S_3 is supplied with square wave and inverted square wave of fundamental frequency, respectively. Fig. 2 presents the gating signals of S_2 and S_4 and it can be observed that T_{ov} is embedded into the

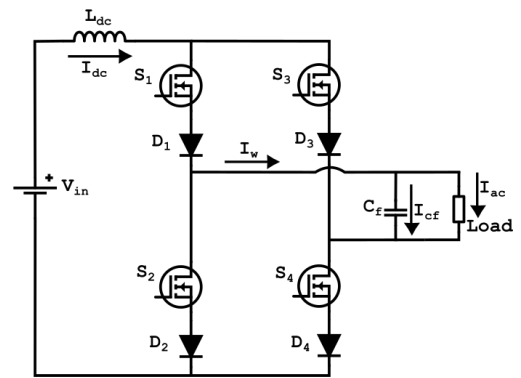


Fig. 1. Single-Phase H-Bridge CSI circuit

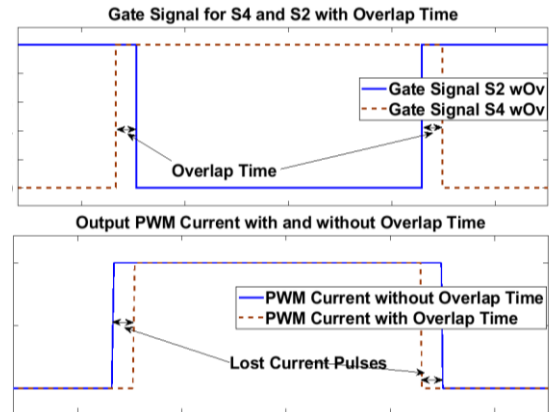


Fig. 2. Gating signals of switches S_2 and S_4 , and output PWM current with and without overlapping

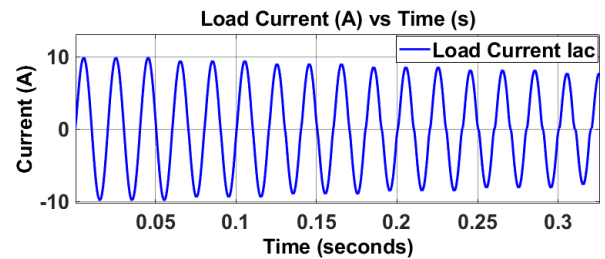


Fig. 3. Effect of increasing the overlapping time on the shape and amplitude of the output AC current (conventional overlapping technique)

gating signals to avoid the open circuit condition. Fig. 2 also depicts the output PWM current with conventional overlapping (I_w) and output PWM current without any overlapping (I_{w0}). During the overlap time, the DC current flows through both switches of one phase simultaneously, bypassing the AC side. As a result, I_w loses current pulses (ΔI_w) and the width of pulses of I_w gets reduced as compared to that of I_{w0} . This reduction in the pulse-width of I_w adversely affects the amplitude of load current/output AC current (I_{ac}) and increases the harmonics in it.

TABLE I. SIMULATION PARAMETERS

Parameter	Value
DC current (I_{dc})	10A
Load resistance (R_{load})	10 Ω
Filter capacitor (C_f)	50 μ F
Switching frequency (f_s)	22kHz
Fundamental frequency (f_f)	50Hz

TABLE II. EFFECT OF OVERLAP TIME ON OUTPUT AC CURRENT AT UNITY MODULATION INDEX (CONVENTIONAL TECHNIQUE)

Overlap Time (μs)	I_{ac} (A)	THD (%)
0	9.871	0.62
1	9.316	2.12
2	8.767	4.35
3	8.221	6.77
4	7.671	9.37
5	7.130	12.08

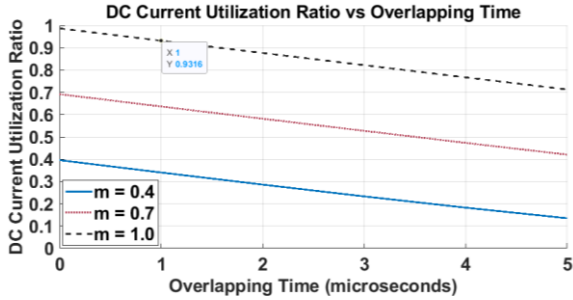


Fig. 4. Effect of increasing the overlapping time on DCUR for different values of modulation index

Table I presents the parameters of the simulated CSI system, which are used for the evaluation of both conventional and proposed overlapping techniques in simulations. Fig. 3 shows the effect of increasing the T_{ov} on the shape and amplitude of I_{ac} when the modulation index (m) is set to 1. Initially T_{ov} is set to $0\mu\text{s}$ and after every three cycles of I_{ac} , it increases by $1\mu\text{s}$. It is clearly visible that as the T_{ov} is increasing, amplitude of I_{ac} is decreasing and deterioration of its shape is increasing, i.e. harmonics in I_{ac} are increasing. Table II presents the amplitude and THD (%) of the output AC current (I_{ac}) against different values of overlap time (T_{ov}) at unity modulation index. It could be noticed that for each increment of $1\mu\text{s}$ in T_{ov} , the amplitude of I_{ac} reduces between 0.54 and 0.55A. Moreover, it could also be observed that with an overlap time of $5\mu\text{s}$, THD exceeds 12%.

DCUR is the ratio between the peak value of fundamental component of output current (I_{o1}) and I_{dc} , as shown in (1). The maximum value of DCUR is equal to m . The relation between DCUR and T_{ov} for three different values of modulation index, i.e. $m = 0.4, 0.7$ and 1 is shown in Fig. 4.

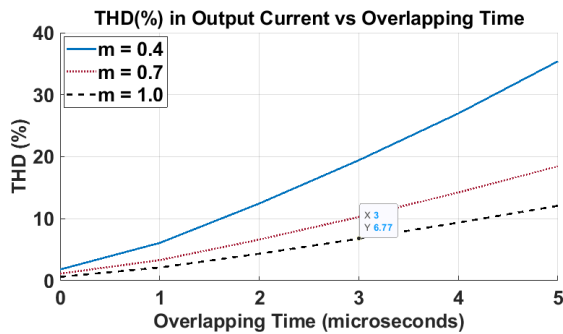


Fig. 5. Effect of increasing the overlapping time on THD (%) of output AC current for different values of modulation index

$$DCUR = \frac{I_{o1}}{I_{dc}} \quad (1)$$

As shown in Fig. 4, DCUR is dependent on both T_{ov} and m . For a fixed value of m , DCUR and T_{ov} have negative linear relationship. It can be observed that the DCUR is low for lower values of m , and its percentage decrease is more with respect to an increasing T_{ov} when the modulation index is low. For $m = 1$, an overlapping of $5\mu\text{s}$ decreases the DCUR by 27.77% (from 0.9871 to 0.7130) compared to the case with no overlapping time. In case of $m = 0.7$, an overlapping of $5\mu\text{s}$ reduces the DCUR from 0.6918 to 0.4205, i.e., by 39.22%, and when $m = 0.4$, it reduces from 0.3957 to 0.1351, i.e., by 65.86%. In case of conventional overlapping technique, lower values of modulation index results in lower DCUR for the same overlapping time which is in accordance with (1).

As shown in Fig. 3 that the deterioration of the shape of I_{ac} and harmonics in it increases with the increase of T_{ov} . Fig. 5 presents the effect of increasing the T_{ov} on the THD (%) of output AC current I_{ac} for different values of modulation index i.e., $m = 0.4, 0.7$ and 1. For $m = 1$, an overlapping of $5\mu\text{s}$ results in 12.08% THD in I_{ac} . In case of $m = 0.7$, same overlapping time generates 18.45% THD (52% more than the previous case) and for $m = 0.4$, THD exceeds 35% when the overlapping time approaches to $5\mu\text{s}$. In case of conventional overlapping technique, lower values of modulation index results in more THD for the same overlapping time.

It can be observed from Fig. 3 that the deterioration of the shape of I_{ac} and harmonics in it increases with the increase of T_{ov} . Fig. 5 shows the effect of increasing T_{ov} on the THD (%) of output AC current I_{ac} for different values of modulation index i.e., $m = 0.4, 0.7$ and 1. For $m = 1$, an overlapping of $5\mu\text{s}$ results in 12.08% THD in I_{ac} . In case of $m = 0.7$, same overlapping time generates 18.45% THD (52% more than the previous case) and for $m = 0.4$, THD exceeds 35% when the overlapping time approaches to $5\mu\text{s}$. In case of conventional overlapping technique, lower values of modulation index results in more THD for the same overlapping time.

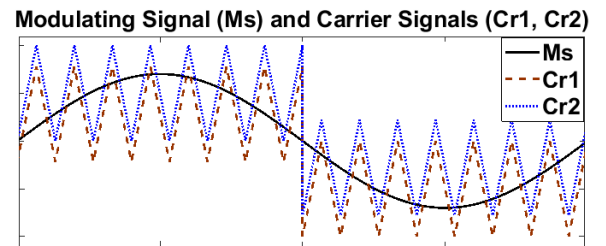


Fig. 6. Proposed carrier-based modified level-shifted modulation technique

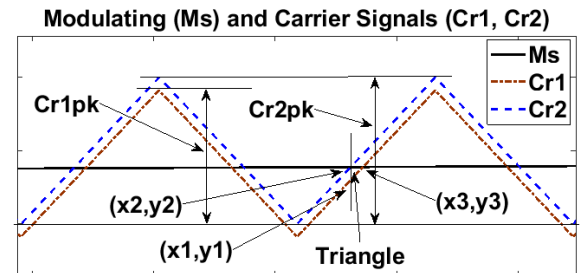


Fig. 7. Modulation and carrier signals of proposed technique (enlarged signals)

B. Proposed overlap time effect suppression technique

This section discusses the proposed overlap time effect suppression method. As shown in Fig 6, the proposed technique employs carrier based SPWM with a modification in the carrier signals. Modulating signal (M_s) is a sinusoidal signal with fundamental frequency (f_f), and carrier signals $Cr1$ and $Cr2$ are triangular signals with a frequency equal to the switching frequency (f_s). For the demonstration purposes, in Fig. 6 the frequency of carrier signals is set to 750Hz, and a level shift of 0.28 is added. As shown in Fig. 7, both carrier signals have equal peak to peak amplitude but peak value of $Cr1$, i.e. $Cr1pk$ is lower than the peak value of $Cr2$ that is $Cr2pk$, due to compensated offset of $Cr1$. This compensation of carrier signals equips the CSI with overlap time effect suppression which allows to retrieve the lost current pulses, improves the DCUR and harmonic performance. The level shift/offset between $Cr1$ and $Cr2$ is denoted by α and it can be calculated by using (2).

$$\alpha = Cr2pk - Cr1pk \quad (2)$$

Both carrier signals have same frequency and peak to peak amplitude, but they have different offset α . This simplifies the establishment of mathematical relation between α and T_{ov} by using trigonometry. Since the overlapping time is much smaller than the period of M_s , M_s could be approximated to a straight line during the overlapping interval. As shown in Fig. 7, during the overlapping M_s intersects $Cr1$ and $Cr2$ which allows to create a right-angle triangle in which perpendicular (vertical distance between both carrier signals) is equal to the value of α and base (horizontal distance between both carrier signals) is equal to T_{ov} . Slope of carrier signals in this region of interest is equal to $2 \cdot f_s$ so $Cr1$ and $Cr2$ could be represented by (3) and (4), respectively.

$$Cr2 = 2 \cdot f_s \cdot x \quad (3)$$

$$Cr1 = 2 \cdot f_s \cdot x - \alpha \quad (4)$$

x represents the time. To make the calculations simple, let suppose one vertex (x_2, y_2) of triangle is at origin. This means M_s will intersect $Cr1$ when it will be equal to zero as $y_3 = y_2$. By putting $Cr1$ equal to zero, (5) is accomplished which shows T_{ov} is directly proportional to α when f_s is kept constant.

$$x = x_3 = T_{ov} = \frac{\alpha}{2 \cdot f_s} \quad (5)$$

As mentioned earlier, the upper switches of both legs (S1 and S3) are provided with square wave and inverted square wave of fundamental frequency as gate signals, respectively, and the lower switches of both legs (S2 and S4) are fed with PWM. Fig. 8 describes the proposed overlap time effect suppression technique in more detail. It presents the modulating signal and carrier signals again to demonstrate the implementation of proposed overlapping technique. The gate signal of switch S4 (GS S4) and gate signal of switch S2 (GS S2) with conventional overlapping (wOv) and proposed overlapping techniques are also presented in Fig. 8. As shown in the figure, equal T_{ov} is added between the GS S4 and GS S2 by using both conventional and proposed techniques. It is clearly visible that the gate signals with conventional

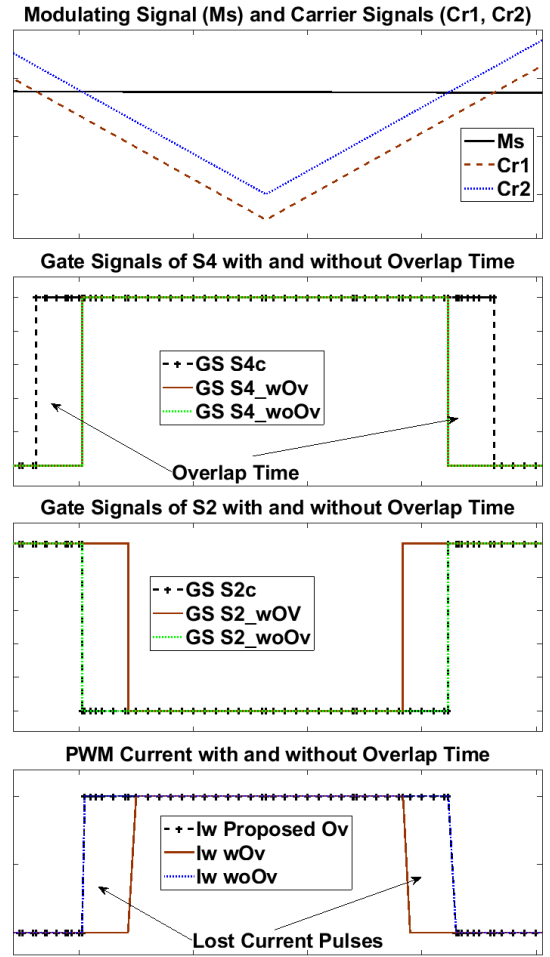


Fig. 8. Proposed overlap time effect suppression technique and conventional technique (enlarged signals)

overlapping technique are different from the gate signals generated with proposed technique. To demonstrate the effectiveness of proposed overlap time effect compensation technique, Fig. 8 also presents the PWM current without any

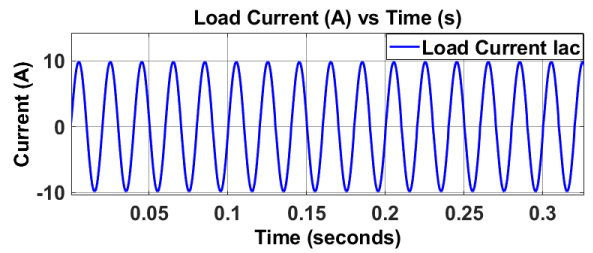


Fig. 9. Effect of increasing overlapping time on (shape and amplitude) load current (proposed overlapping technique)

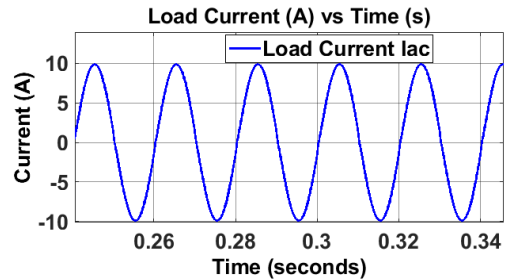


Fig. 10. Enlarged load current (proposed overlapping technique)

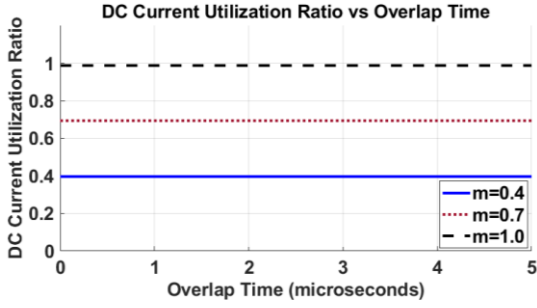


Fig. 11. Effect of increasing overlapping time on DCUR for different values of modulation index

TABLE III. EFFECT OF OVERLAP TIME ON OUTPUT AC CURRENT AT UNITY MODULATION INDEX (PROPOSED TECHNIQUE)

Overlap Time (μs)	I_{ac} (A)	THD (%)
0	9.871	0.62
1	9.873	0.91
2	9.874	1.28
3	9.875	1.59
4	9.875	1.86
5	9.875	2.06

overlapping (I_w woOv), PWM current generated with conventional overlapping technique (I_w wOv) and PWM current generated with proposed compensation technique (I_w Proposed Ov). It is clearly visible that the conventional overlapping technique loses pulses of current (ΔI_w) which reduces the width of its PWM current I_w wOv as well as DCUR and increases the harmonics content in AC load current. However, the proposed technique produces the PWM current I_w Proposed Ov which is equally wider as the PWM current produced without any overlapping (I_w woOv) due to recovery of the lost current pulses (ΔI_w). This recovery of lost current pulses results in a lot of benefits i.e. it significantly improves the DCUR and harmonic performance of CSI.

The AC current waveform with different values of overlapping time is shown in Fig. 9. It shows the effectiveness of proposed technique by presenting the effect of increasing the T_{ov} on the shape and amplitude of I_{ac} when m is set to 1. Initially T_{ov} is set to $0\mu s$ and after every three cycles of I_{ac} , it increases by $1\mu s$. It is clearly visible that increase in T_{ov} has no significant effect on the amplitude of I_{ac} . Table III presents the amplitude and THD of the output AC current (I_{ac}) against different values of overlap time (T_{ov})

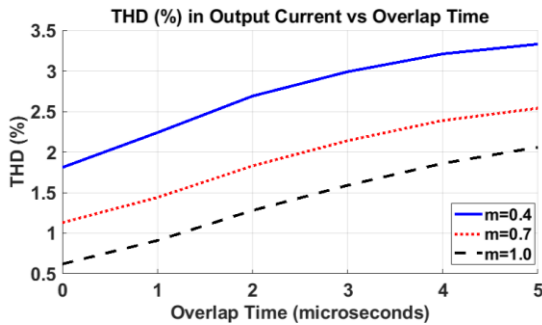


Fig. 12. Effect of increasing overlapping time on THD (%) of output AC current for different values of modulation index

at unity modulation index. It could be noticed that with a variation of T_{ov} from $0\mu s$ to $5\mu s$, the amplitude of I_{ac} increases by $0.004A$ instead of decreasing, which indicates that the lost current pulses are fully recovered as shown in Fig. 8. Fig. 10 presents the enlarged signals of I_{ac} with $4\mu s$ and $5\mu s$ overlap time.

To validate the performance of proposed technique, Fig. 11 presents the DCUR versus overlapping time for three different values of m , i.e. 0.4, 0.7 and 1. It can be observed that DCUR is no more varying with the variation of T_{ov} and it is only dependent on m . The higher values of m will result in higher DCUR, however there is no noticeable variation in DCUR when T_{ov} is varied from $0\mu s$ to $5\mu s$. For $m = 1$, DCUR is equal to 0.9871 when there is no overlapping. As T_{ov} is increased from $0\mu s$ to $5\mu s$, DCUR changes from 0.9871 to 0.9875, which is an increase of 0.04%. Whereas, with conventional overlapping technique this was reduced by 27.77%. With $m = 0.7$ and 0.4, DCUR varies from 0.6918 to 0.6922 and from 0.3957 to 0.3959 respectively, as T_{ov} is varied from $0\mu s$ to $5\mu s$.

There is a slight deterioration in the shape of I_{ac} due to effect of increasing T_{ov} , which is hard to notice from Fig. 9 and Fig. 10. Fig. 12 shows how the THD of output AC current I_{ac} is affected by increasing T_{ov} for different values of modulation index, i.e. $m = 0.4, 0.7$ and 1. Similar to conventional overlapping technique, THD of output current with proposed technique increases with the increase of T_{ov} , and lower values of modulation index result in higher THD for the same value of overlap time, but proposed technique significantly limits this. For $m = 1$, an overlapping of $5\mu s$ results in 2.06% THD in I_{ac} which is almost six times lower than the case of conventional overlapping technique. In case of $m = 0.7$, an overlap time of $5\mu s$ generates 2.54% THD which is seven times lower than the case of conventional overlapping technique. Similarly for $m = 0.4$, the same overlapping of $5\mu s$ results in 3.33% THD which is 10.6 times lower than the THD produced in case of conventional overlapping technique.

C. Fourier analysis of output AC current

The output AC current waveform with an overlapping time of $5\mu s$, presented in Fig. 9, has a small unsymmetry as the maximum appears slightly above $\frac{\pi}{2}$.

An approximation of curve of the output current in (6)

$$i_{ac}(t) = \begin{cases} a \sin(\omega t - b \sin(\omega t)) & \text{for } \omega t \leq \pi \\ a \sin(\omega t + b \sin(\omega t)) & \text{for } \omega t \geq \pi \end{cases} \quad (6)$$

Since $i_{ac}(t)$ is a periodic signal so it can be expressed by a Fourier series of the form presented in (7).

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos(n\omega t) + b_n \sin(n\omega t) \quad (7)$$

Where

$$a_n = \frac{2}{T} \int_{t-T}^t f(t) \cos(n\omega t) dt \quad (8)$$

$$b_n = \frac{2}{T} \int_{t-T}^t f(t) \sin(n\omega t) dt \quad (9)$$

T is the fundamental period. Each harmonic component can be expressed by its magnitude (h_n) and phase (δ_n).

$$h_n = \sqrt{a_n^2 + b_n^2} \quad (10)$$

$$\delta_n = \arctan\left(\frac{a_n}{b_n}\right) \quad (11)$$

Since the output AC current shown in Fig. 9 is a pure AC signal so $a_0 = 0$. Because of the complexity of $f(t)$ the Fourier analysis are performed using MATLAB-Simulink simulations. To validate the presented analysis, THD of output ac current is estimated by using the $f(t)$ when $m = 0.7$ and overlapping time is $5\mu s$. The simulation results give 2.06% THD in the output AC current of CSI when the maximum frequency of 550Hz is used for THD computation. The THD computed through $f(t)$ is also 2.06%. In both cases, the even harmonic components are all zero: $h_2 = h_4 \dots = 0$, and only odd harmonic components are found in the output current and $f(t)$. The magnitude and phase of odd harmonics estimated through Fourier analysis are presented in Table IV.

TABLE IV. FOURIER ANALYSIS RESULTS

Harmonic Order n	$h_n(A)$	$\delta_n(^{\circ})$
1	6.92	-1.89
3	0.137	87.8
5	0.033	90
7	0.015	90
9	0.0089	90
11	0.0059	90

III. EXPERIMENTAL RESULTS

To validate the effectiveness of proposed overlap time effect suppression technique, CSI circuit shown in Fig. 1 is developed by using CREE C3M0075120K MOSFETs, CREE C4D05120 schottky diodes and 50uF capacitor. Toroid AA-98023 transformer is used a DC link inductor and its primary side is connected in series with the DC voltage source to create a DC current source. The proposed compensation technique is implemented in dSPACE to control the CSI. Experimental setup is presented in Fig. 13. To analyze the performance of the proposed technique, experiments are carried out with 5V input, 22 Ω load

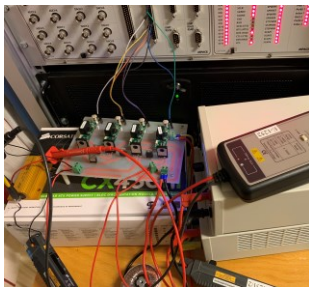


Fig. 13. Experimental setup

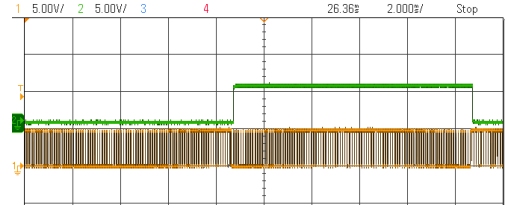


Fig. 14. Gate signals of switches S1 and S4

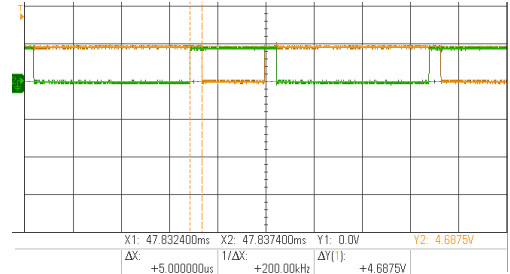


Fig. 15. Gate signals of switches S2 and S4

resistance, 10kHz switching frequency, 0.9 modulation index and an overlapping time of $5\mu s$.

The gate signals of switches S1 and S4 are shown in Fig. 14, whereas Fig. 15 presents the gate signals of switches S2 and S4 which have an overlap time of $5\mu s$. Fig. 16 shows the DC link current and output AC current of CSI. It could be observed that DC current is continuous and switching ripples are very low, but second order harmonic of fundamental frequency is dominant which has peak to peak amplitude closer to 10% of average DC link current. AC current has a nice sinusoidal shape. However, there is a small amount of switching ripples on its peaks, but it does not have any even order harmonic as shown in Fig. 17. It does not have the distortion near zero crossing which was there in case of conventional overlapping technique, as shown in Fig. 3. The proposed technique has diminished the effect of overlap time

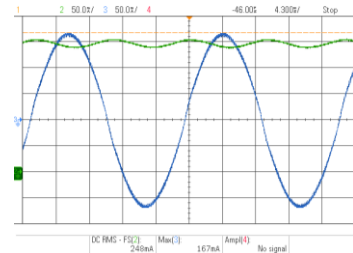


Fig. 16. DC current and output AC current

and has

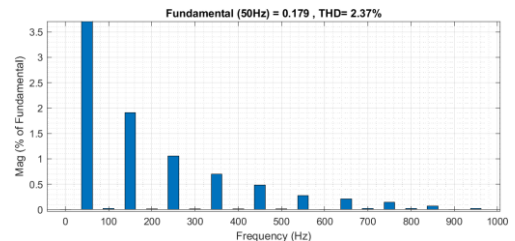


Fig. 17. Measured THD(%) of output AC current

significantly improved the quality of AC current. THD(%) and relative magnitudes of harmonics are presented in Fig. 17. THD(%) in the output current is 2.37% which is in conformance with the curves presented in Fig. 12 and all the harmonic components have magnitudes less than 2%. The highest magnitude is of third harmonic which is equal to 1.9%

whereas, fifth and seventh harmonic components have magnitudes of 1.05% and 0.69%, respectively.

IV. CONCLUSIONS

Overlap time is essential for the reliable operation of CSI, but insertion of it significantly decreases the DCUR, deteriorates the shape of AC current and increases the harmonics. These issues significantly affect the performance of CSI, so suppression of overlap time effect is vital. This paper proposes and discusses a novel technique to mitigate the overlap time effect. The proposed technique equips the carrier based SPWM with an overlap time effect suppression by using modified level shifted carrier signals. It fully recovers the lost current pulses, thus significantly reduces the THD of output AC current and improves the DCUR, and it remains constant for increasing overlapping time. A mathematical relation between the level shift and overlap time is established, and a function to approximate the AC current is also presented. The proposed technique is evaluated with MATLAB-Simulink simulations, and results are compared with the conventional overlapping technique. Moreover, experimental test results are also presented to validate the effectiveness of proposed overlap time compensation technique. The experimental results verify the simulation results; thus, it could be concluded that proposed technique has mitigated the effect of overlap time, significantly reduced the THD and improves the DCUR of CSI. In future, experimental setup will be tested with slightly high voltage and current and analysis of its DCUR will be carried out.

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